Research Migration Project

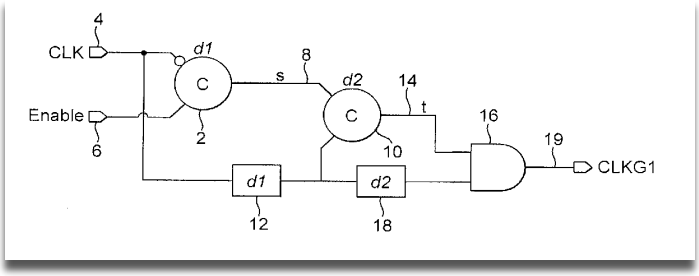
Name of the participant : Thejesh Varma Vulchu

Title of the circuit : Glitch-Free Clock Gating Circuit using Dual Muller C-Elements

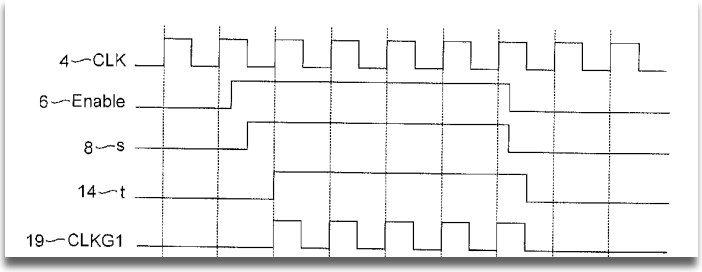
Theory: The **Glitch-Free Clock Gating Circuit** is an advanced power-management architecture that uses the asynchronous logic of **Muller C-elements** to safely disable the clock signal to inactive digital blocks. In high-speed digital systems, standard clock gating often relies on simple AND gates, which are prone to producing "glitches" or "runt pulses" if the Enable signal toggles during a clock transition; these tiny voltage spikes can cause metastability, data corruption, or total system failure. This circuit is critical because it introduces a "**rendezvous**" **synchronization** mechanism where the output state is only updated when both the clock and the enable signal have reached a stable, matching state, effectively *filtering out any hazardous transitions*. By employing a dual-stage Muller gate structure, the design ensures that even asynchronous Enable signals from different clock domains are perfectly aligned with the main clock pulses, providing a robust, speed-independent solution that maintains signal integrity while significantly *reducing dynamic power consumption*.

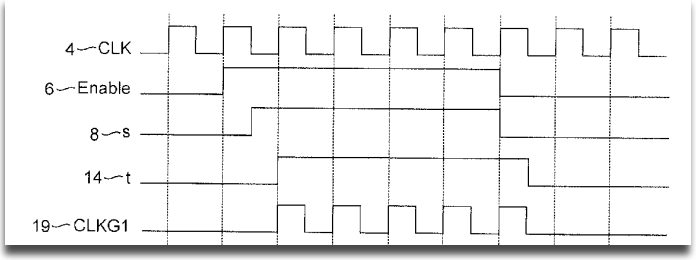
Working Principle: The working principle of this circuit is based on asynchronous rendezvous logic that synchronizes an Enable signal with the clock to prevent partial pulses. The **first Muller gate** receives an inverted clock and Enable signal to ensure the gating window only opens when the clock is low. A **second Muller gate** re-synchronizes this window with the delayed main clock to *eliminate signal racing and timing jitter*. Strategic delay elements are used to compensate for the internal propagation time of the gates, ensuring perfect alignment at the final logic output. The resulting gated clock output only toggles at full cycle widths, providing a glitch-free, power-efficient solution for high-speed digital systems.

Circuit Diagram(s) :



Expected Results (Input, Output waveforms) :





Source/Reference(s) :1. Patent EP2515197A1: "Clock gating circuit using a Muller C-element," STMicroelectronics.

2. A Design of a Fast and Area Efficient Multi-Input Muller C-element