Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

**Name of the participant :** Bellana Venkata Chaitanya

Title of the circuit : Design of Single Precision Floating Point Arithmetic Logic Unit

Theory/Description : —Floating point numbers are used in many applications such as telecommunications,medical imagining,radar,ete.In top-down design approach,four arithmetic modules,addition, sub traction,multiplication and division are combined to form a floating point ALU unit.Each module is independent to each other.In this paper,the implementation of a floating point ALU is designed and simulated.This paper presents the design of a single precision floating point arithmetic logic unit.The operations are performed on 32-bit operands.The algorithms of addition,subtraction,division and multiplication are modeled in Verilog HDL using ModelSim and an efficient algorithm for addition and subtraction module is developed in order to reduce the no.of gates used.The RTL code is synthesized using Synopsys RTL complier for 180nm TSMC technology with proper constraints. Keywards-floating point number,FPU,overflow.underflow, exceptions,normalization,ete.

Circuit Diagram(s) :
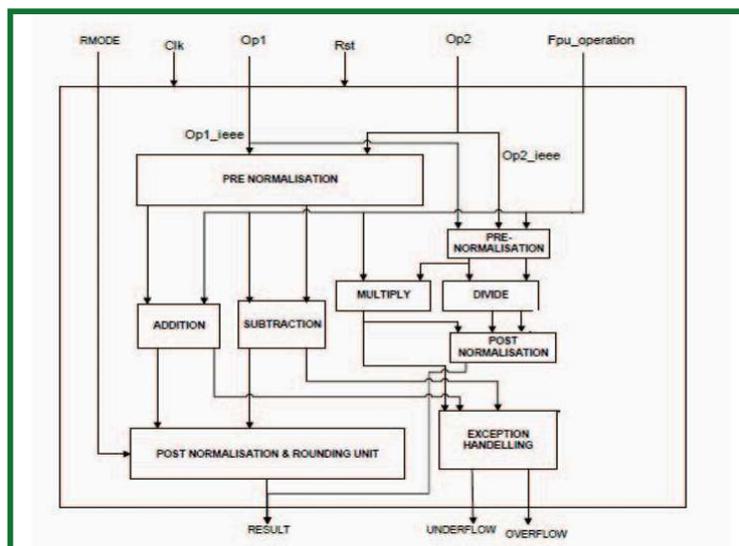
Results :
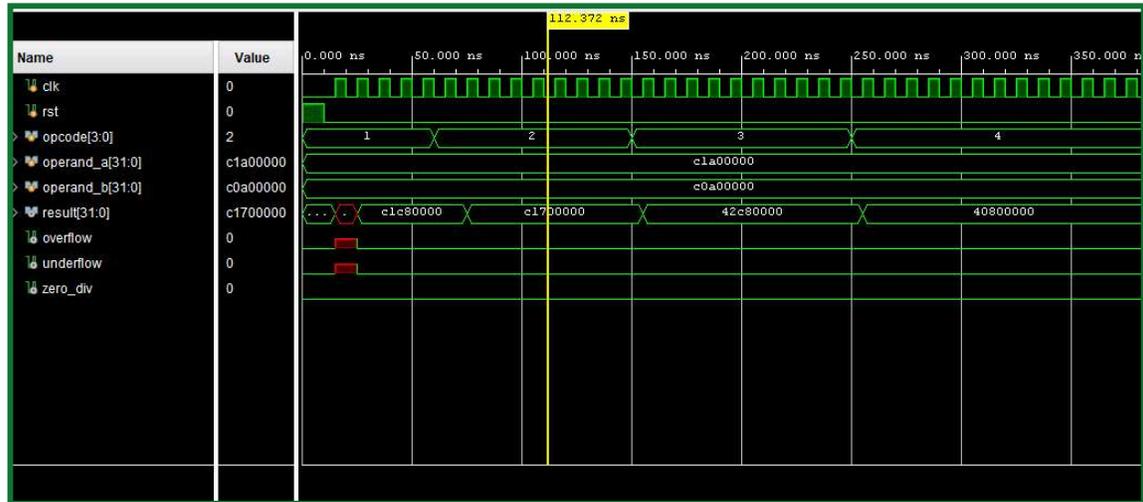
Source/Reference(s) :

[1]Shanthala.N1,Nayana.M,Chandrashekar.C, Dr.Siva Yellampalli"Basic operation Performed on Arithmetic Lope Unit (ALU)For 32-Bit Floating Point Numbers",International Joumal of Applied Engineering Research ISSN 0973 4562 Volume 12,Number 12 (2017)pp.3248-3252 Research India Publications. http://www.ripublication.com

 [2]Swathi.A,G.Sirinivasulu"ASIC Implementation of a High Speed Double Presicion(64 bitf)Floating Point Unit using verilog", International Journal and Magazine of Engincering,Technology, Management and Research ISSN 2348-4845