Circuit Simulation Project

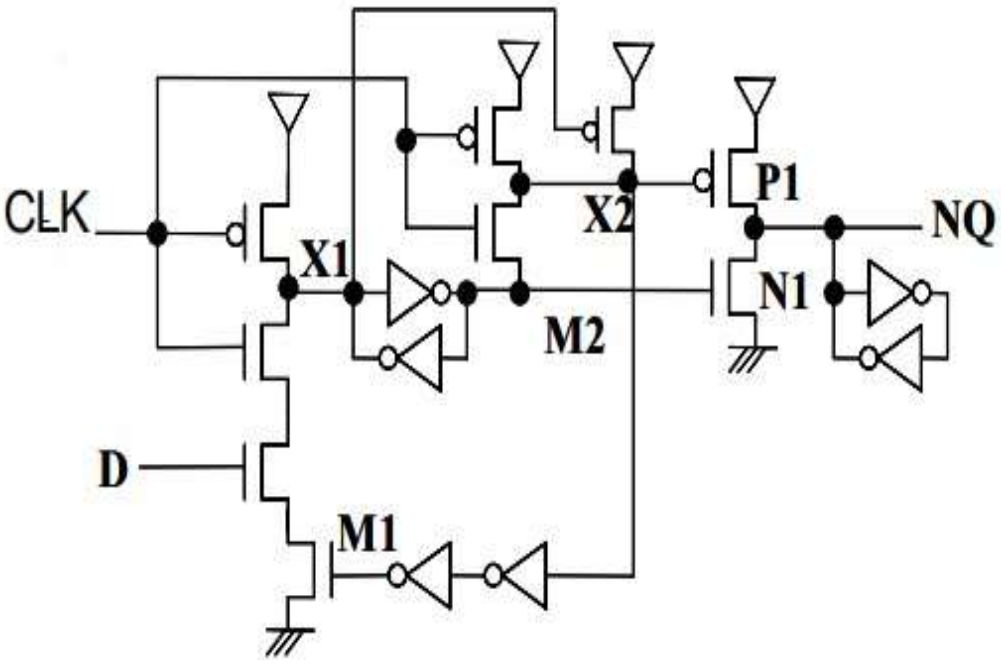
https://esbn.fossee.tn/ctrcuit-simutatton-project

name of the participant: S.Pandigarajan

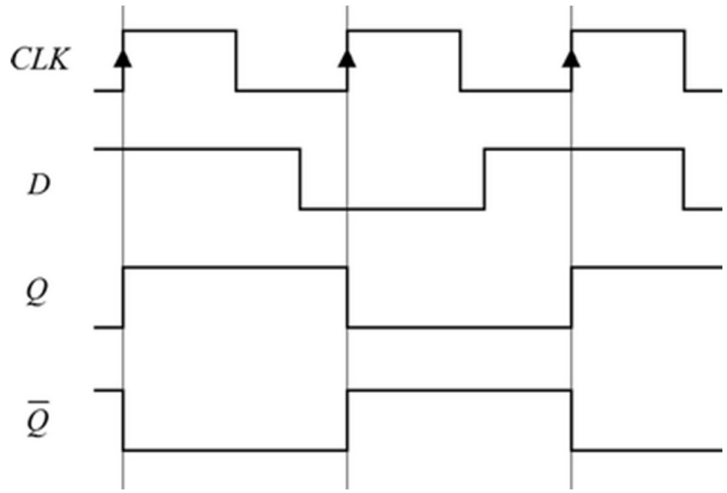
Titte of the circuit: Cross Charge Control Flip Flop using Esim

Theory/Deccription: The Cross Charge-Control Flip-Flop (XCFF) is a low-power dynamic flip-flop that uses an implicit internal pulse to capture data during clock transitions. XCFF reduces power by splitting the dynamic storage into two independent nodes, so only one node switches per clock cycle, lowering overall switching activity and clock loading.However, XCFF can experience unwanted precharge at internal nodes X1 and X2, especially during long sequences of repeated '1's or '0's. This occurs due to the conditional shut-off mechanism, which increases hold-time requirements during the clock's 0→1 transition and may occasionally cause incorrect output transitions.Despite this limitation, XCFF is widely used for low-power, high-speed VLSI designs.

Circuit Diagram(s)



Results (Input, Output waveforms and/or Multimeter readings):



Source/Reference(s):

Titte of the Paper: Performance Evaluation of Pulse Triggered Flip flops in 32 nm COWS Regime

name of the journal/Publication: IEEE Solid State Circuits Author(s): A.Hirata, K.Nakanishi, M.Nozoe and A.Miyoshi.

Chapter Volume Pages: 306-307, 16-18 JUNE 2005

Link: https://ieeexplore.ieee.org/document/10141264