

TITLE: Design and optimize a 4×4 multiplier for speed and efficiency

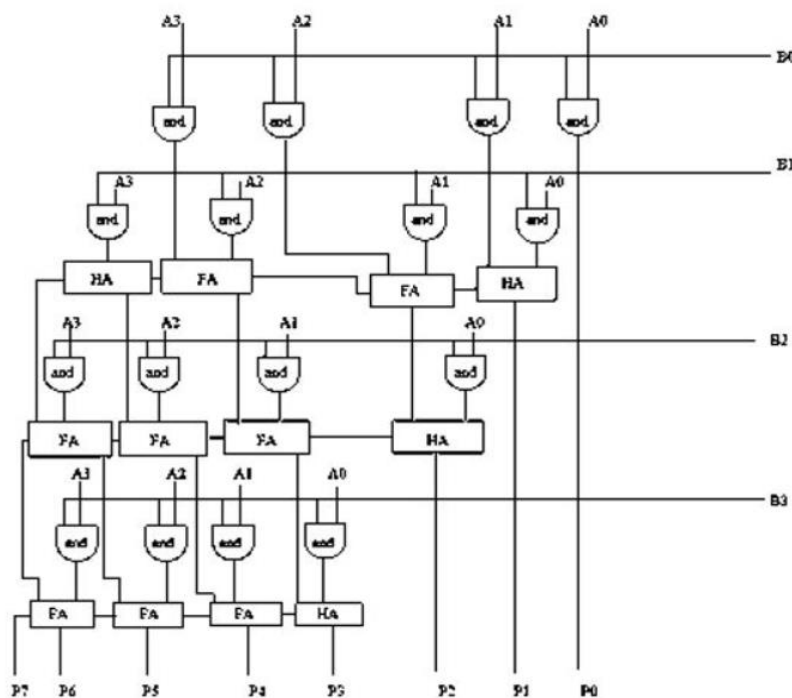
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PROBLEM STATEMENT

Design and implement a 4×4 multiplier circuit that achieves high speed, low power consumption, and efficient hardware utilization. The goal is to optimize partial product generation and addition to minimize propagation delay and complexity, making the circuit suitable for real-time applications in digital signal processing, embedded systems, and VLSI designs.



JOURNAL/PUBLICATION DETAILS

REFERENCE:

1. <https://www.elprocus.com/4x4-array-multiplier-and-its-working/>
2. <https://www.jetir.org/papers/JETIRDC06021.A>
3. eSim FOSSEE – IIT BOMBAY

