Circuit Simulation Project

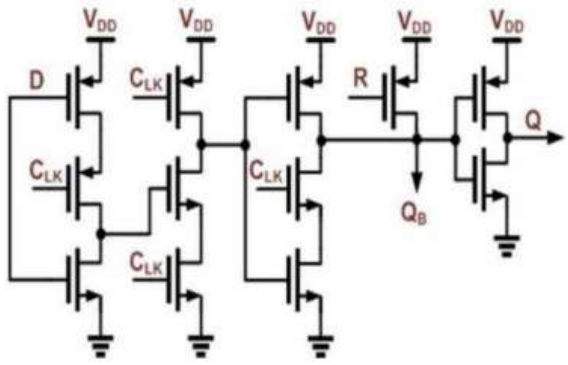
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Pandiyarajan.S

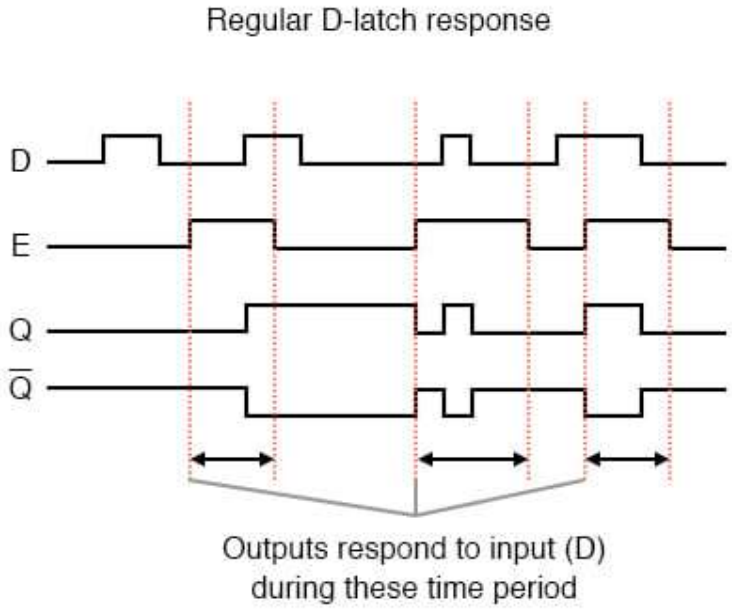
Title of the circuit : TSPC Based D Flip Flop

Theory/Description : The True Single-Phase Clock (TSPC) flip-flop offers low-power and high-speed operation by using only one clock phase across all stages. Our design implements a negative-edge triggered architecture with non-precharged N, precharged P, and non-precharged P stages, along with reset logic, requiring a total of 12 transistors. The circuit reliably captures data on the falling clock edge, making it suitable for CMOS high-speed applications. However, as a dynamic latch-based structure, it is limited to MHz-range operation due to leakage issues at very low frequencies.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :



Source/Reference(s) :

Title of the Paper: Setup and Hold Time Analysis of D Flip-Flop based on CMOS and GNRFET

Name of the Journal/Publication: IEEE Paper

AUTHOR(S): ShrutiShrivastava, Usha Chauhan, Mohammad Rashid Ansar

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LINK: https://ieeexplore.ieee.org/document/10150117