Circuit Simulation Project

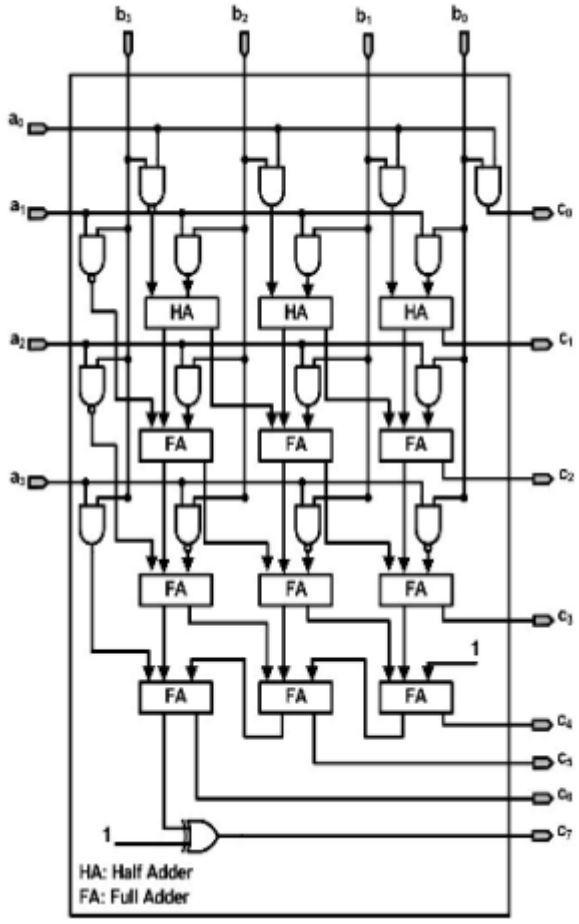
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Jovin P John

Title of the circuit : 4-bit Baugh-Wooley Multiplier

Theory/Description : A 4-bit Baugh-Wooley multiplier is a circuit that directly multiplies two 4-bit signed numbers without separate sign handling. It uses a grid of logic gates and adders arranged systematically to generate the 8-bit product result. This design efficiently handles negative numbers using two's complement arithmetic in hardware.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

a	b	Output (Product)
1111	1111	11100001
1110	1110	11000100
1101	1101	10101001
1100	1100	10010000
1011	1011	01111001
1010	1010	01100100
1001	1001	01001001
1000	1000	01000000
0111	0111	00110001
0110	0110	00100100
0101	0101	00011001
0100	0100	00010000
0011	0011	00001001
0010	0010	00000100
0001	0001	00000001
0000	0000	00000000

Source/Reference(s) : Puttaswamy, M., Premananda, B. S., & Kamat, N. (2024). Area and energy optimized Hamming encoder and decoder for nano-communication. Journal of Electrical Engineering