Circuit Simulation Project

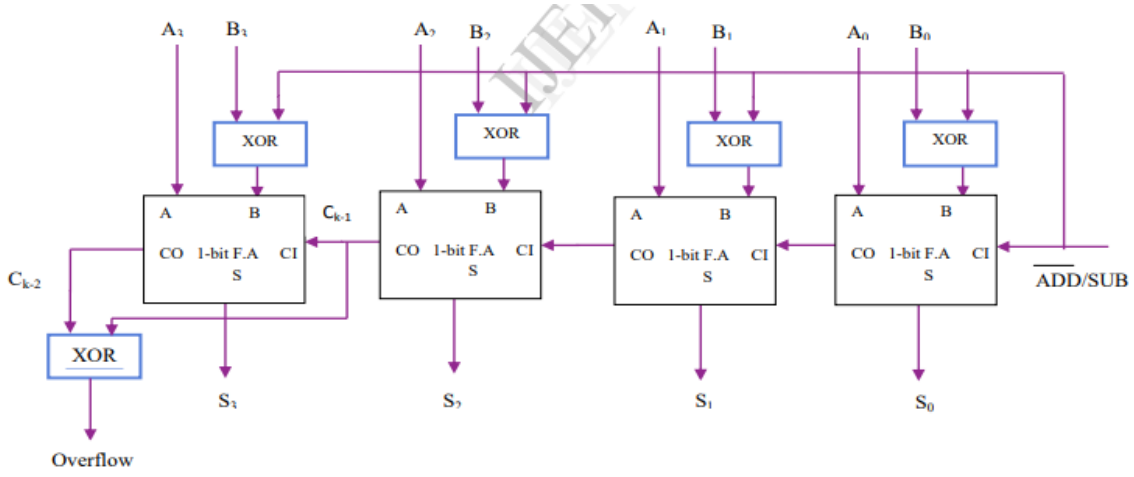
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Jovin P John

Title of the circuit : 4-bit 2's Complement Adder/Subtractor

Theory/Description : A 4-bit 2's Complement Adder/Subtractor is a circuit that can do both addition and subtraction on 4-bit numbers. It uses a control signal to switch between the two operations and works with signed numbers using the 2's complement method.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

A	B	AS	S3	S2	S1	S0	OVF
1111	1111	1	0	0	0	0	0
1110	1110	0	1	1	0	0	0
1101	1101	1	0	0	0	0	0
1100	1100	0	1	0	0	0	0
1011	1011	1	0	0	0	0	0
1010	1010	0	0	1	0	0	1
1001	1001	1	0	0	0	0	0
1000	1000	0	0	0	0	0	1
0111	0111	1	0	0	0	0	0
0110	0110	0	1	1	0	0	1
0101	0101	1	0	0	0	0	0
0100	0100	0	1	0	0	0	1
0011	0011	1	0	0	0	0	0
0010	0010	0	0	1	0	0	0
0001	0001	1	0	0	0	0	0
0000	0000	0	0	0	0	0	0

Source/Reference(s) : Ajitha, D., Kumar, P. Y., Ramanaiah, K. V., & Sumalatha, V. (2013). Efficient design of 2's complement adder/subtractor using QCA. *International Journal of Engineering Research & Technology (IJERT)*, 2(11), 1–4. ISSN: 2278-0181.