Circuit Simulation Project

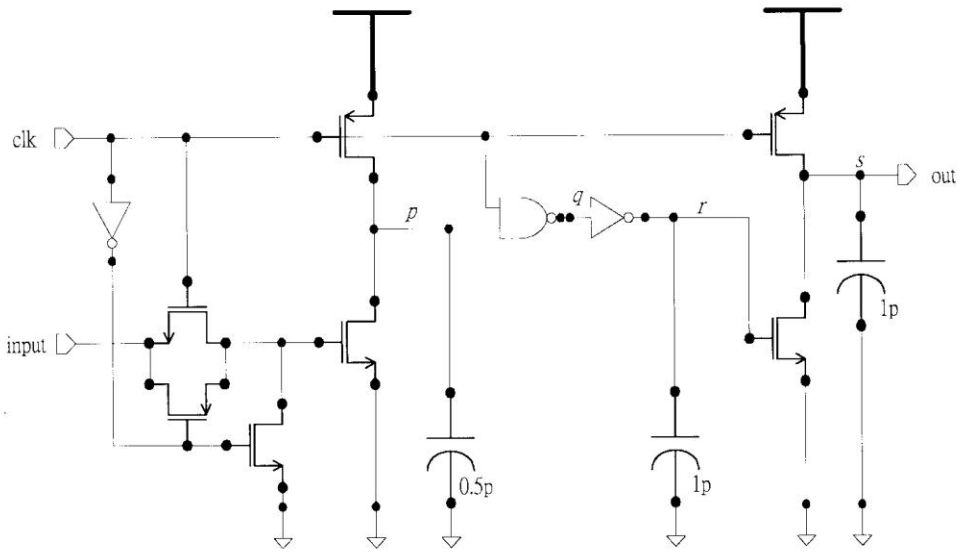
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Gowtham M

Title of the circuit : A Low-Power and High-Speed Dynamic PLA Circuit Configuration for Single-Clock CMOS

Theory/Description : Existing PLA styles all trade speed for power or signal quality: pseudo-NMOS is easy but wastes static power and needs big transistors, dynamic NOR-NOR can glitch unless you slow it with a delayed clock, domino logic saves power yet long NMOS strings add delay and cause charge sharing, Dhong's precharged OR/charge-sharing AND loses full voltage swing and still needs a delayed clock, and Blair's pseudo-NMOS NOR shortens paths but leaks static power and drives loads poorly. Adding a buffering NAND between two NOR planes sidesteps these issues by removing the ground switch, shrinking power spikes and preventing races while still using a single clock.

Circuit Diagram(s) :



Low-power and high-speed PLA circuit.

Results (Input, Output waveforms and/or Multimeter readings) :

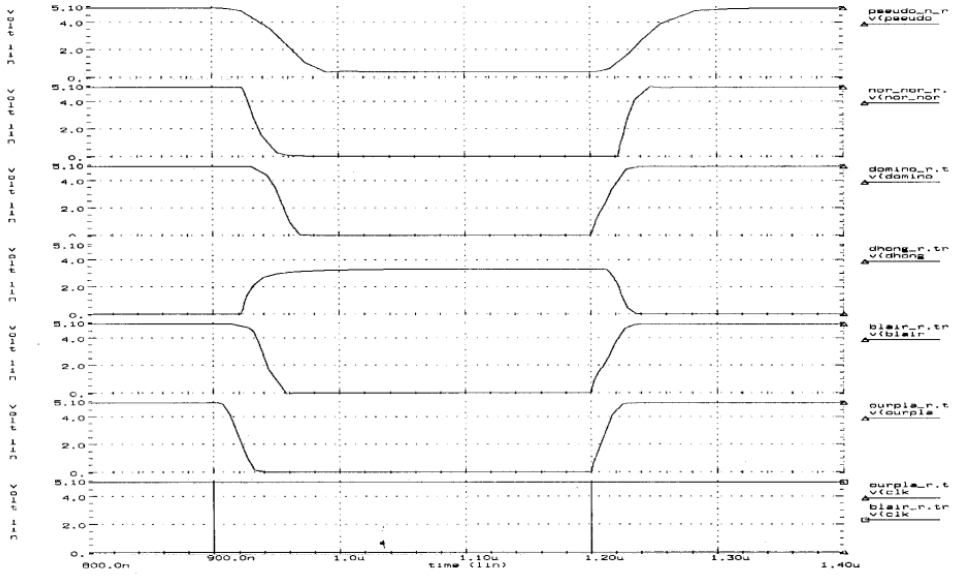


Fig. 3. Waveforms of PLA design alternatives.

Source/Reference(s) :

Title of the Paper : A Low-Power and High-Speed Dynamic PLA Circuit Configuration for Single-Clock CMOS

Name of the Journal : IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I

Reference : Wood, Roy A., et al. "An electrically alterable PLA for fast turnaround-time VLSI development hardware." *IEEE Journal of Solid-State Circuits* 16.5 (2003): 570-577**.**