IMPLEMENTATION OF 4-BIT RIPPLE CARRY ADDER USING OPTIMIZED 10T FULL ADDER IN ESIM

Problem Statement:

In the research paper *"**Design, Simulation and Comparative Analysis of CMOS Ripple Carry Adder**"*, two Full Adder designs and two 4-bit Ripple Carry Adder (RCA) designs are analyzed. A major limitation identified is the **high transistor count** in conventional CMOS implementations. Specifically, a standard CMOS Full Adder requires **28 transistors**, which results in a **4-bit RCA needing 112 transistors**. This high transistor count leads to:

- **Increased chip area**, making the design less efficient for VLSI applications.
- **Higher power consumption**, which is critical for battery-powered and low-power devices.
- **Longer propagation delay**, since the carry must ripple through each stage, affecting overall speed.

Although the paper demonstrates some improvement in area and power for one of the Full Adder designs, the fundamental challenges of **excessive transistor usage and carry propagation delay** remain. These issues limit the scalability of conventional RCAs when designing higher-bit adders.

Proposed Solution:

To overcome the limitations of conventional CMOS 4-bit Ripple Carry Adders, we propose the design and implementation of a **4-bit RCA using optimized 10-transistor (10T) Full Adders**. The proposed solution focuses on:

1. **Reduced Transistor Count:** Each Full Adder uses only **10 transistors**, reducing the total count for the 4-bit RCA from **112 to 40 transistors**.
2. **Lower Power and Area:** Fewer transistors lead to **less power consumption** and **smaller chip area**, making the design suitable for low-power VLSI applications.
3. **Improved Performance:** Efficient carry logic minimizes propagation delay, improving the **overall speed of the adder**.
4. **Simulation and Verification Using eSim:** The 4-bit RCA will be designed and simulated using **eSim software** for schematic-level verification and performance evaluation.

The 10T-based RCA provides a **scalable, low-power, and area-efficient alternative** to conventional CMOS designs.