Circuit Simulation Project

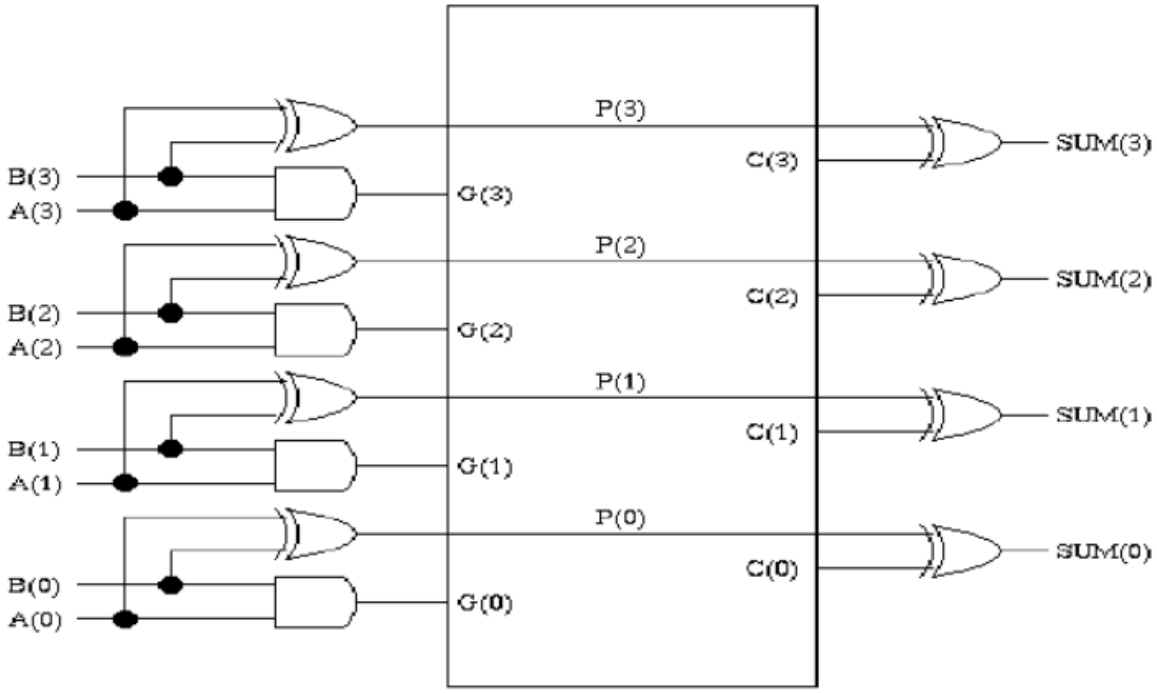
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Jovin P John

Title of the circuit : 4-bit Carry Lookahead Adder

Theory/Description : A 4-bit Carry Lookahead Adder (CLA) is a fast digital adder that improves speed compared to ripple carry adders. Instead of waiting for each carry to propagate, it uses generate and propagate signals to calculate carries in parallel. This reduces delay and makes addition faster, especially for larger bit-widths. The CLA is widely used in processors where high-speed arithmetic operations are required.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

A	B	Cin	Sum	Cout
1111	1111	1	1111	1
1110	1110	0	1100	1
1101	1101	1	1011	1
1100	1100	0	1000	1
1011	1011	1	0111	1
1010	1010	0	0100	1
1001	1001	1	0011	1
1000	1000	0	0000	1
0111	0111	1	1111	0
0110	0110	0	1100	0
0101	0101	1	1011	0
0100	0100	0	1000	0
0011	0011	1	0111	0
0010	0010	0	0100	0
0001	0001	1	0011	0
0000	0000	0	0000	0

Source/Reference(s) : Kumar, R., & Dahiya, S. (2013). Performance analysis of different bit carry look ahead adder using VHDL environment. *International Journal of Engineering Science and Innovative Technology (IJESIT)*, 2(4), 1–5. ISSN: 2319-5967.