TITLE : Simulation of Six-Stage Linear CMOS Charge Pump with Complementary Clocking

STUDENT NAME : PRAVIN A

COLLEGE NAME : Sri Eshwar College of Engineering

PROBLEM STATEMENT :

The demand for compact and efficient voltage conversion circuits has grown significantly in low-power and portable electronic devices. Traditional inductive converters increase size and complexity due to inductors. Charge pumps offer an inductorless solution for voltage multiplication and inversion using switched capacitors and MOSFET switches. However, issues such as voltage ripple, output current limitation, and device threshold voltage losses affect performance. This project designs and simulates a six-stage CMOS charge pump circuit using complementary PMOS and NMOS switches, aiming for efficient voltage boosting in a compact layout. The design must ensure non-overlapping clock operation to maximize charge transfer and minimize energy loss. Performance evaluation focuses on output voltage level and ripple.

ABSTRACT :

This paper presents the design and simulation of a multi-stage CMOS charge pump circuit for efficient voltage multiplication without the use of inductors. The circuit employs complementary PMOS and NMOS switches controlled by non-overlapping clock signals to achieve stepped-up DC output voltage suitable for low-power integrated applications. Key design challenges addressed include minimizing voltage ripple, overcoming threshold voltage drops, and optimizing switch timing to enhance charge transfer efficiency. The capacitive charge storage and transfer mechanism allows for a compact and highly integrable solution for portable electronic devices. Simulation results demonstrate stable voltage gain and low output ripple across multiple stages. The design is validated using modern device models to ensure compatibility with current CMOS fabrication processes. This charge pump architecture provides a practical on-chip voltage boosting.

PROPOSED CIRCUIT :

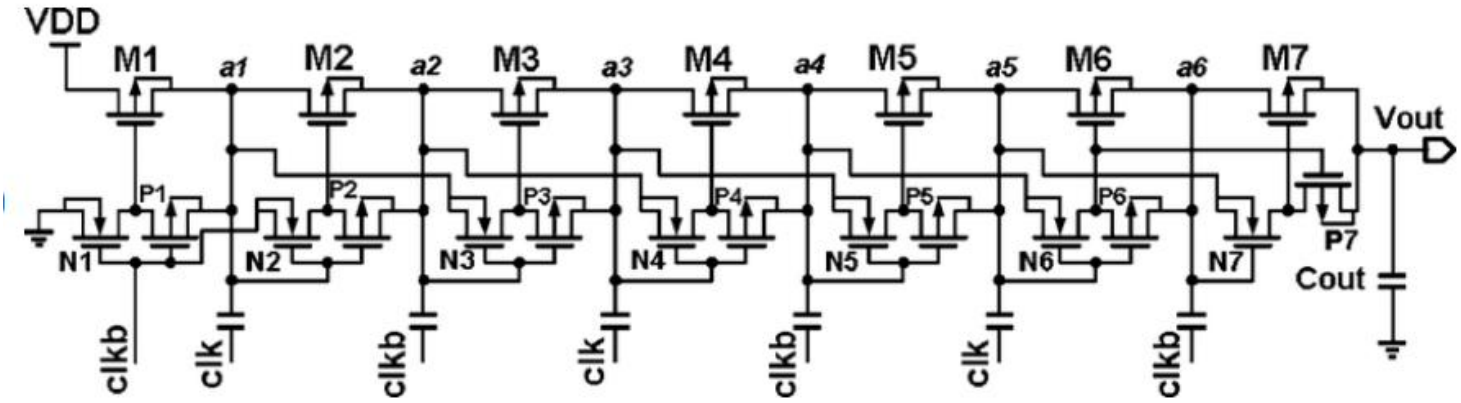

Fig 1 : Six-Stage Linear CMOS Charge Pump

REFERENCES :

[1] D. Heo, “Six-stage linear charge pump circuit with all PMOS switches,” ResearchGate, 2021. [Online]. Available: https://www.researchgate.net/figure/Six-stage-linear-charge-pump-circuit-with-all-PMOS-switches-13_fig3_262605123.

[2] Ryan Perigny, et al., "Area Efficient CMOS Charge Pump Circuits," Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), 2001.