Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

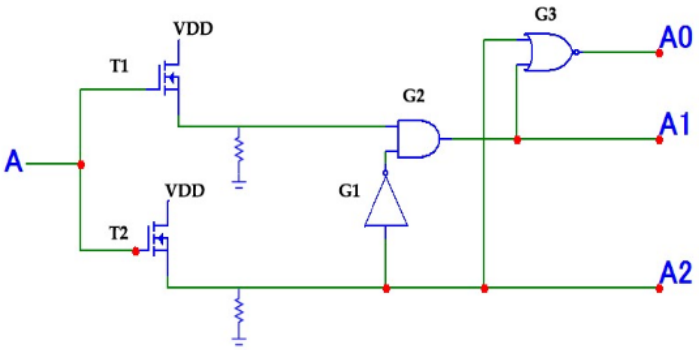
Name of the participant : NEERAJ G

Title of the circuit : Ternary Decoder Using CMOS DPL Binary Gates using Esim

Theory/Description :

Most modern digital devices are constructed with two-valued logic circuits that have only two representations (0, 1) associated per wire. The performance of these systems relies on how fast these valued states can change. However, as demand for systems with a higher efficiency, speed, and lower power consumption rise, the attention on multiple-valued logic (MVL) systems has been growing. MVL lodges greater amount of information per wire than binary circuits providing less interconnections and thus a simpler circuit structure. The resulting circuit has a smaller area, less power dissipation, and better performance. Of the MVL systems, ternary logic (base-3) is the most investigated and has a balance of complexity and efficiency. In a ternary logic system, each digit (trit) may receive three values (0, 1, 2), with a corresponding voltage for each value. For example, the decimal number 234 uses 8 binary bits but can be represented with 5 ternary trits. The amount of information is compact and efficient. Therefore, circuit designs using ternary logic could yield great potential for VLSI and future digital circuits.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

Ternary Input (A)	T1 Vth= 0.7v	T2 Vth= 1.4v	Binary Output		
			A0	A1	A2
Logic **0** (0v)	Open	Open	**1(1.8V)**	**0**	**0**
Logic **1** (0.9v)	Close	Open	**0**	**1(1.8V)**	0
Logic **2** (1.8v)	Close	Close	**0**	**0**	**1(1.8V)**

Source/Reference(s) :

Title of Paper: A Novel Implementation of Ternary Decoder Using CMOS DPL Binary Gates

Name of the journal/publication: IEEE Solid State Circuits

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Link: https://ieeexplore.ieee.org/document/8672698