Circuit Simulation Project

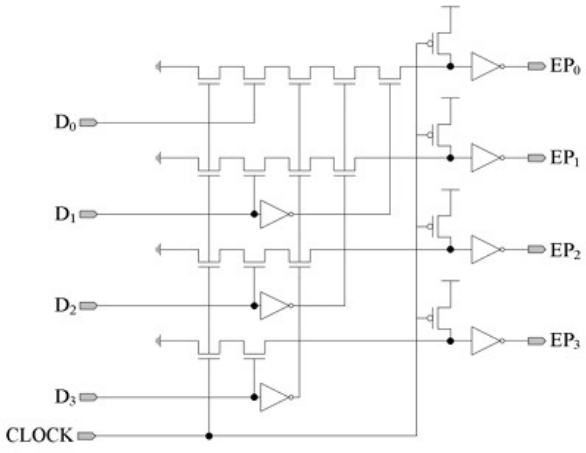
https://esim.fossee.in/circuit-simulation-project

Name of the participant : SHYLASH.S

Title of the circuit : A Full Parallel Priority Encoder Design Using Esim

Theory/Description : Priority encoders and comparators represent fundamental components in modern digital system design. A priority encoder generates an output that specifies the position of the highest-priority input bit asserted to logic "1," thereby facilitating efficient data interpretation. Such encoders are frequently employed in comparators, which are responsible for determining the relative magnitude of two digital inputs. The performance of a comparator is directly influenced by the speed and efficiency of its priority encoder. Conventional NAND-gate–based encoder architectures suffer from longer critical paths, thereby limiting high-speed operation. Earlier approaches, such as the 4-bit model proposed by Wang et al., demonstrated functional capability but were unsuitable for high-performance comparator applications. Subsequent CMOS-based priority encoder designs achieved performance improvements while maintaining manageable circuit complexity. The introduction of parallel MSB checking comparators further reduced delay compared to NAND-type implementations, yet the critical path delay remained a significant concern. To address these limitations, the concept of a Full Parallel Priority Encoder (FPPE) has been proposed. This design aims to enhance comparator efficiency by eliminating serial NAND-type delays, thereby offering superior performance for high-speed digital systems.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

TABLE I
Results of proposed comparator

A_{big}	B_{big}	Result Indicates
0	0	A = B
0	1	A < B
1	0	A > B
1	1	Not allowed

Source/Reference(s) :

Title of the Paper: A Full Parallel Priority Encoder Design Used In Comparator

Link: https://ieeexplore.ieee.org/document/5548664