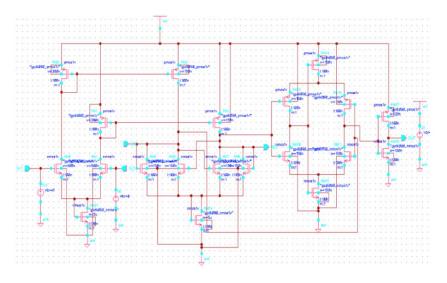# Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant : JITHESHKRISHNA R
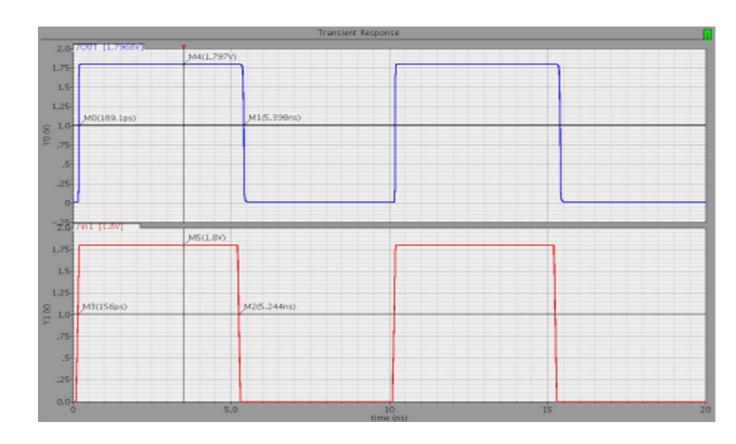
Title of the circuit : Transient analysis of three-stage comparator using esim

Theory/Description : A comparator is an electronic circuit that compares two analog signals and produces a digital output, making it functionally similar to a one-bit analog-to-digital converter (ADC). Comparators are essential components in many applications such as ADCs, level shifters, relaxation oscillators, window detectors, and null detectors. This paper focuses on the design and analysis of a three-stage conventional comparator that consists of a preamplifier stage, a decision-making stage, and an output buffer stage. The proposed comparator is implemented using 90-nm CMOS technology with the Cadence Virtuoso software (gpdk90 library). Along with the design, the paper evaluates and compares the performance parameters of three types of comparators: the conventional comparator, the latch-based comparator, and the hysteresis-based comparator. The discussion includes background information, circuit design, operational details, and simulation results. The work aims to demonstrate improvements and trade-offs in comparator design for high-speed and high-precision applications**.**

Circuit Diagram(s) :

Results (Input, Output waveforms and/or Multimeter readings) :

Source/Reference(s) :