RESEARCH MITIGATION PROJECT

Name: Harshini Ganga T S

Title of the circuit: Implementation of AND Gate using Transmission Gates

College: SSN College of Engineering

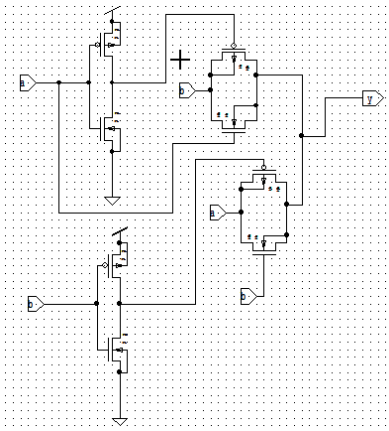
Problem Statement:

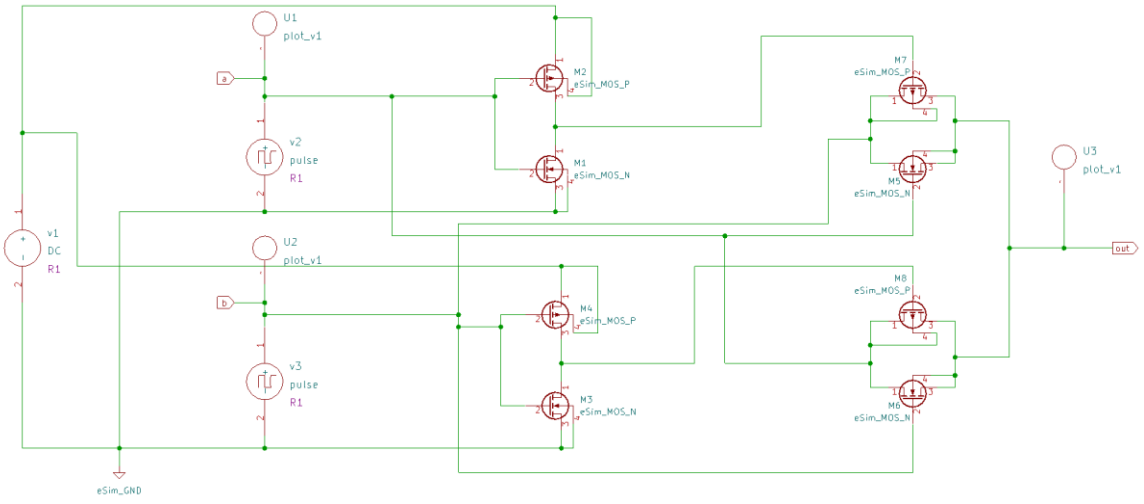
This project presents the design and simulation of an AND gate using Transmission Gates in eSim to achieve efficient and simplified logic implementation. The design leverages the switching capability of TR gates to minimize transistor usage and power consumption, making it suitable for low-power VLSI applications.

Description:

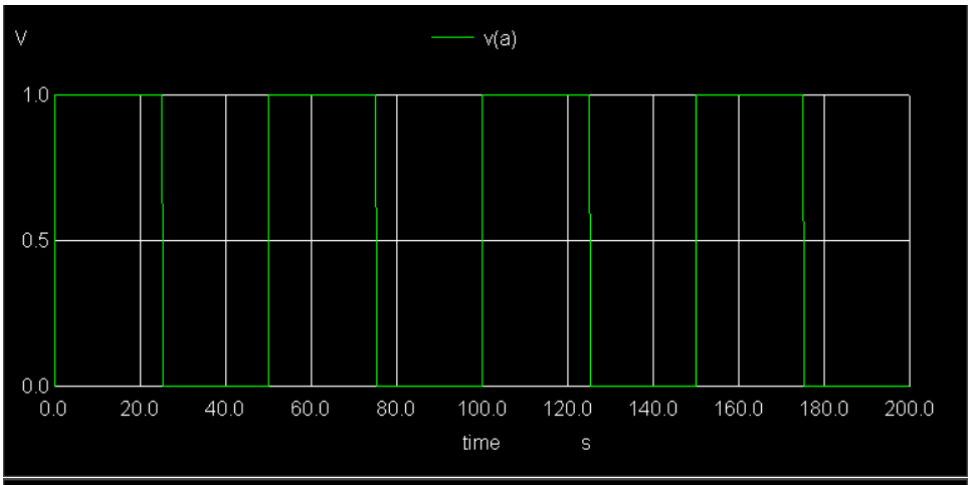
A Transmission Gate (TR gate) is a bidirectional switch made of parallel NMOS and PMOS transistors controlled by complementary signals, allowing both logic '0' and '1' to pass without degradation. It is widely used in digital design for multiplexers, latches, and low-power circuits. Using this property, an AND gate can be implemented by allowing input A to pass through the TR gate only when control input B is high, producing logic '1' only when both inputs are high. When B = 0, the TR gate is off, and the output remains at logic '0'. This design reduces transistor count and power consumption compared to conventional CMOS logic, making it efficient for low-power VLSI applications.

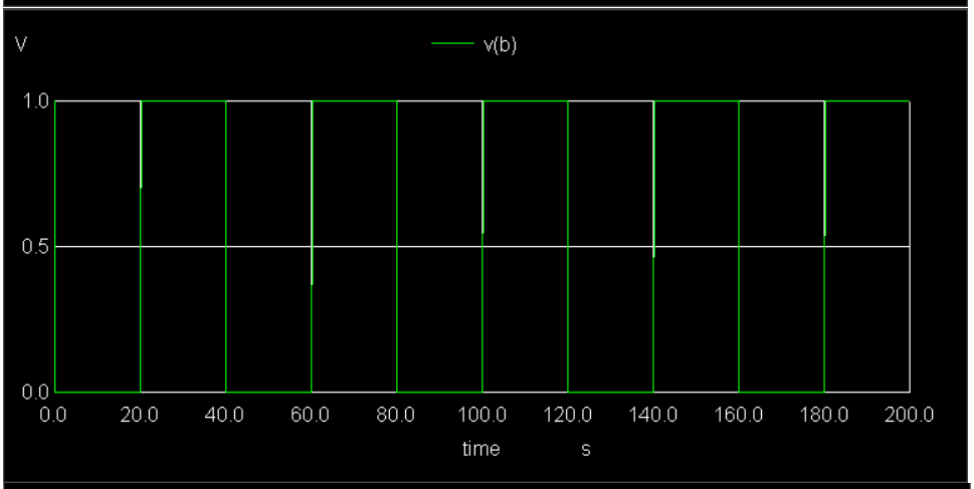
Circuit Diagram and Schematic Diagram:

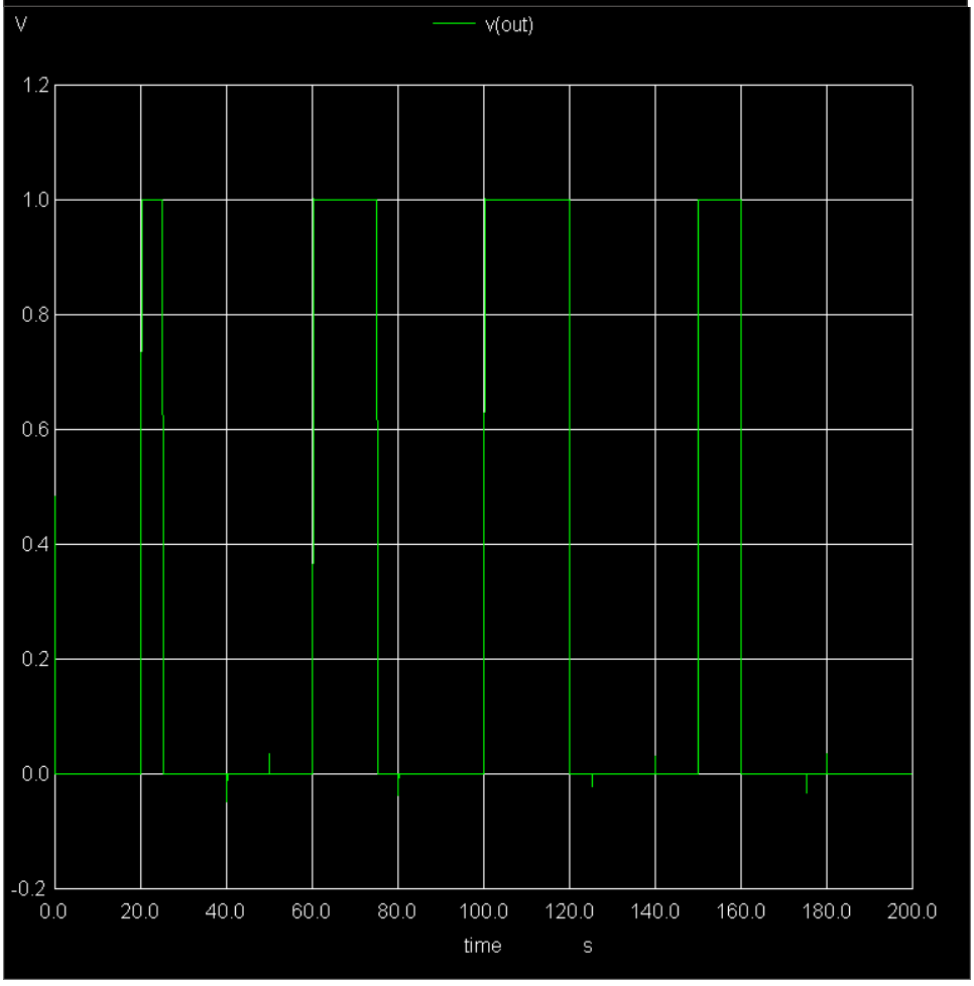




Output:


V
v(a)
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
s


V
v(b)
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
s


V
v(out)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
s

References:

Name of the publication: Combinational Circuits Using Transmission Gate Logic For Power Optimization

Authors: G.Naveen Balaji , V.Aathira, K. Ambhikavathi, S. Geethiga, R. Havin

https://www.researchgate.net/publication/304353741_COMBINATIONAL_CIRCUITS_USING_TRANSMISSION_GATE_LOGIC_FOR_POWER_OPTIMIZATION