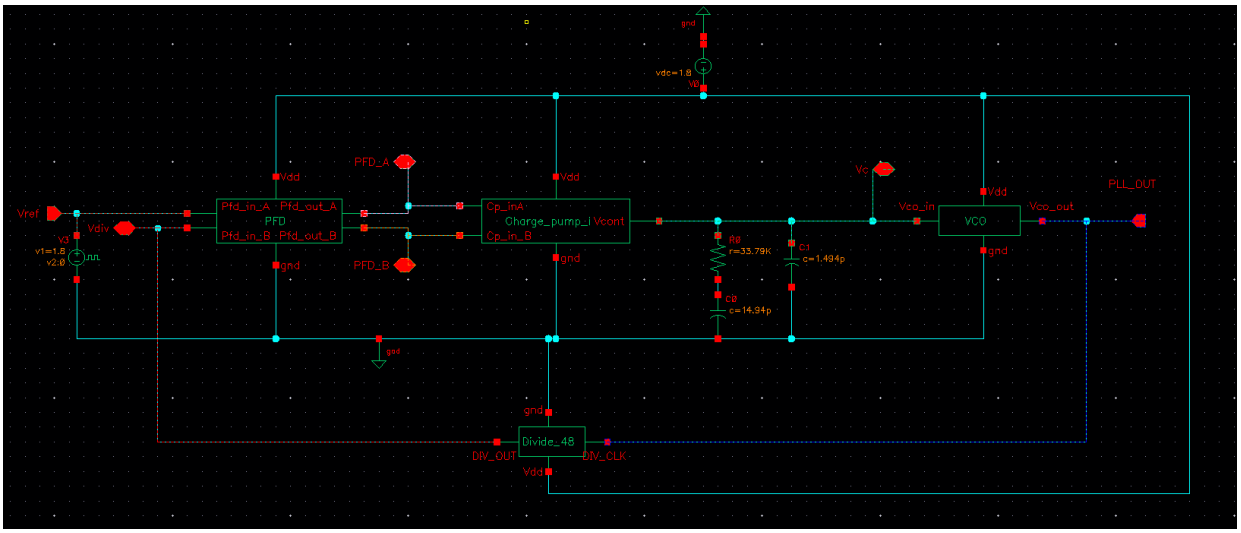
RESEARCH MIGRATION PROJECT

NAME : Karri Pavan

Title of the circuit : Type - II -3rd Order Classical Phase Locked Loop

Theory : This project focuses on the design and implementation of a Type-II third-order classical phase-locked loop (PLL), a high-performance control circuit widely used for frequency and phase synchronization in communication and instrumentation systems. The Type-II architecture incorporates two integrators in its control loop, enabling it to maintain zero steady-state error when tracking both phase and frequency changes, while the third-order loop filter extends system stability and noise suppression capabilities. This combination allows the PLL to achieve rapid locking, broad frequency acquisition range, and excellent resilience against interference, making it ideal for demands in radio transmitters, clock recovery circuits, frequency synthesizers, and precision measurement equipment. The project delivers systematic design methodology, simulation validation, and practical insights into advanced PLL applications, demonstrating the superior tracking, stability, and noise rejection of third-order Type-II PLLs for modern electronic systems

Circuit Diagram :



Source / Reference : https://github.com/madanee20340-droid/Type-II-3rd-Order-Classical-PLL/blob/main/COMPLETE%20PLL.docx