A Highly Linear Low Power Envelop Detector

https://esim.fossee.in/circuit-simulation-project

Name of the participant : Priyanka

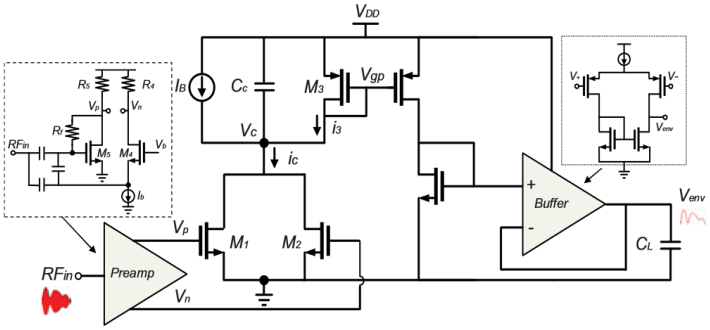
Institutions : Dronacharya group of institutions

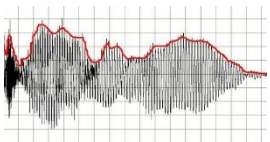
Title of the circuit : Low Power Envelope detector

Branch: Electronic and communication Engineering ngineering

Theory/Description :

Envelope detection is an enabling technique in contemporary communication and sensing systems used extensively in low-power radios, wireless transceivers, biomedical monitoring, and power amplifiers used for envelope tracking. With communication standards like LTE and 5G requiring broader bandwidths and greater linearity, traditional rectifier-based envelope detectors struggle to keep up due to limited speed, limited linearity, and high power consumption. To bypass these limitations, CMOS-based linear detectors offer a lucrative alternative by taking advantage of the quadratic I–V behavior of MOSFETs. Not only do such designs obtain accurate envelope extraction over a broad frequency range, but integration with current RF front-ends at low cost is also possible. In this regard, a very linear and power-efficient envelope detector is proposed that can accurately track wideband modulated signals with limited energy overhead, proving to be applicable to future wireless and portable systems.





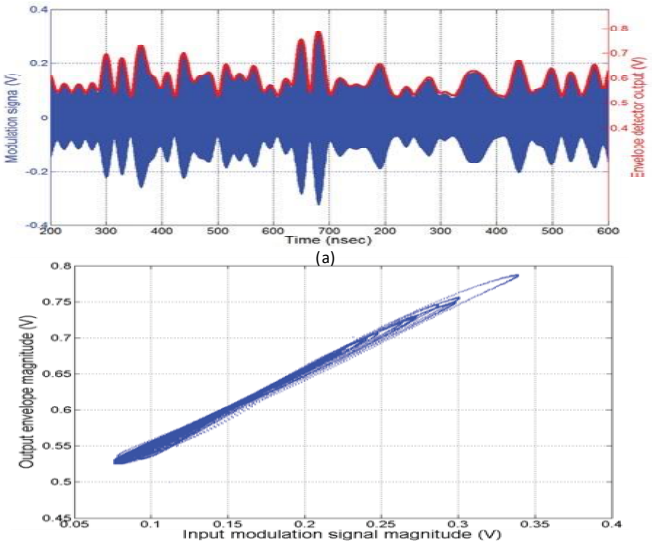
Circuit Diagram and output waveform

Working : Using a CG–CS preamplifier, the circuit first amplifies the RF input before applying it to two MOSFETs, which use their quadratic I–V characteristic to produce a current proportional to the envelope of the signal. After filtering out high-frequency components,

the current is transformed into a clean envelope voltage by a MOSFET that is saturated. The detected envelope is then delivered to the output by a buffer with low power consumption and high linearity

Results :

Using a 0.18 µm CMOS process, the suggested envelope detector tracks a 120 MHz LTE signal at a 3 GHz carrier frequency with little distortion, demonstrating high linearity and wideband performance. The circuit uses only 18 mW of static power, of which the detection core uses about 4 mW, and runs on a 1.8 V supply. Simulation results validate the output envelope's suitability for low-power, wideband, and portable wireless applications by confirming that it follows the input signal closely and accurately.



Conclusion : The low-power envelope detector design proposed here is a power-aware architecture that achieves an effective trade-off between accuracy, bandwidth, and power consumption. Using its standard process technology for integrated circuits in CMOS technology, it has demonstrated the capability to track and detect wideband signal shapes without distortion and at very low power consumption levels, paving the way for possible implementations in real-world applications, such as wireless communications, biomedical tracking and monitoring, and low-power IoT devices. Its compatibility with open-source eSim tools has greatly contributed to its reproducibility and likely efficacy, which leaves it positioned for inclusion into next-generation low-power RF systems.

Source/Reference(s) :

1. Yi-bo Su, Qin Xia, Li Geng, and Xin-Ke Liu, "A Highly Linear Low Power Envelope Detector," IEEE, 2019.
   - This is the main source (your uploaded paper) that explains the CMOS-based highly linear, low-power envelope detector design and simulation results.
2. Richard Lyons, "Digital Envelope Detection: The Good, the Bad, and the Ugly," 2016.
   - This reference discusses various digital envelope detection methods (half-wave, full-wave, square-law, Hilbert transform, etc.), showing broader applicability in communication and biomedical systems.