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Title of Proposed Work:
Design and Simulation of an Inverting R-2R Ladder DAC using eSim

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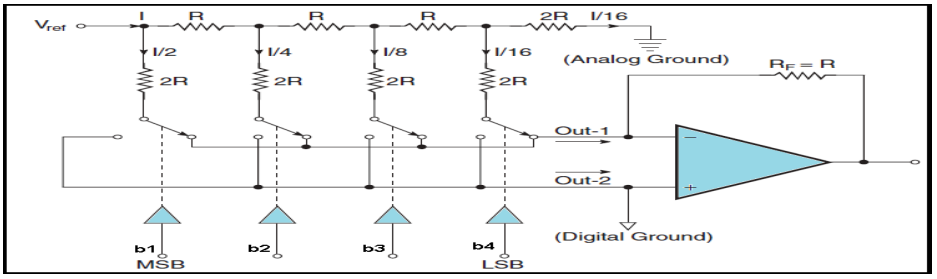
Problem Statement

Digital-to-Analog Converters (DACs) are fundamental circuits in mixed-signal systems, enabling digital systems to interface with the analog world. Traditional DAC implementations such as binary-weighted resistor DACs suffer from high resistor spread requirements, making them impractical for higher resolutions. The R-2R ladder DAC is a widely used architecture that simplifies resistor requirements to just two values (R and 2R).

However, most implementations focus on voltage-mode outputs. This project proposes the design and simulation of an **Inverting R-2R Ladder DAC** that directly interfaces with an op-amp summing amplifier to achieve a negative analog output proportional to the applied digital code. The work will explore step linearity, resistor mismatch effects, and buffering using eSim (ngspice). This will provide practical exposure to DAC design, current summing concepts, and mixed-signal system simulations.

Implementation Plan

- Construct a **4-bit inverting R-2R ladder** using resistor values (R = 10 kΩ, 2R = 20 kΩ).
- Interface ladder output with an **op-amp summing amplifier** configured as an inverting buffer.
- Simulate digital codes (0000–1111) and verify output voltage steps.
- Analyze **linearity (DNL/INL)**, resistor mismatch tolerance, and effect of op-amp parameters.
- Extend design to an **8-bit DAC** and explore scaling and performance trade-offs.



Reference

1. https://www.researchgate.net/publication/3952642_Resistors_layout_for_enhancing_yield_of_R-2R_DACs
2. https://patents.google.com/patent/CA2544873A1/en
3. Title: A CMOS R-2R Ladder Digital-to-Analog Converter Design and Analysis
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