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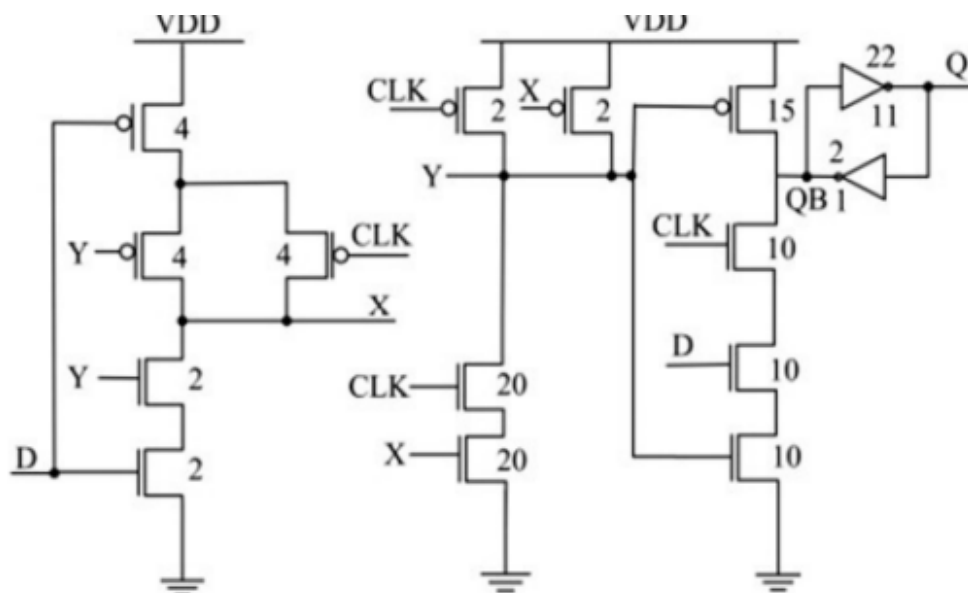
Circuit Simulation Project

Name of the participant : PANDI YARAJAN S

Title of the circuit : Pulse Generator-Free hybrid Latch Based Flip Flop using e-sim

Theory/ Description : Flip-flops (Ff) are key storage elements in digital CMOS circuits, consuming up to 50% of system power through storage and clock networks. Pulse-triggered flip-flops (P-Ff) are preferred over master-slave Ff due to lower power, reduced area, and better performance. This work compares six advanced P-FF designs for power, delay, and efficiency across different voltages and temperatures.

Circuit Diagram(s):



Results (Input, Output waveforms and/ or Multi-meter readings) :

Source/ Reference(s) :

Jinn Wang, Po-Hui Yang, and Duo Sheng "Design of a 3-V

300-MHz low-power 8-b/spl times/ 8-b pipelined multiplier using pulse-triggered TSPC flip-flops," IEEE J. Solid-State Circuits, vol. 35, no. 4, pp. 583–592, Apr. 2000, doi: 10.1109/4.839918.