

Circuit Simulation Project

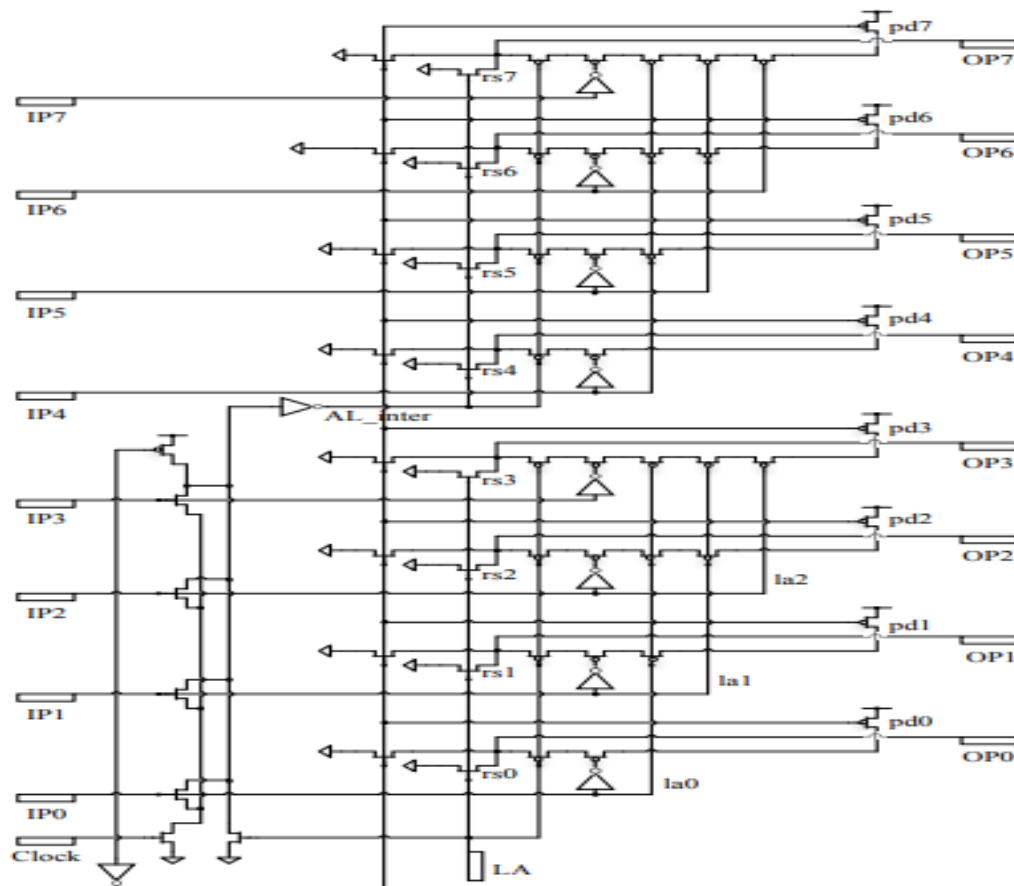
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Title of the circuit : 8-bit cmos priority encoder

Theory/Description : A **priority encoder** is a fundamental digital circuit that encodes multiple input lines into a binary output, assigning priority to the highest-order active input. In particular, an **8-bit CMOS priority encoder** accepts eight input signals and generates a 3-bit binary output along with a valid indicator. Such encoders are widely used in interrupt controllers, processor design, communication systems, and digital signal processing, where multiple simultaneous requests must be resolved efficiently.

The design and analysis of a CMOS-based priority encoder are crucial due to the trade-offs between **power, delay, and scalability** in modern VLSI systems. This work focuses on the **analysis and implementation of an 8-bit priority encoder using CMOS logic**, aiming to optimize performance while maintaining robustness against race conditions and glitches. By modeling the circuit in SPICE and analyzing its behavior across different operating conditions, the study will provide insights into delay, power consumption, and functional correctness. This forms the foundation for extending the design to larger encoders and integrating them into complex digital architectures.

Circuit Diagram :



- Reference/Source :**
1. X. Wang and Y. Feng, "Analysis and Design of 8-Bit CMOS Priority Encoders," arXiv preprint, arXiv:1806.01443, June 2018. [Online]. Available: <https://arxiv.labs.arxiv.org/html/1806.01443>
 2. N. H. E. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., Addison-Wesley, 2011.
 3. M. M. Mano, Digital Design, 5th ed., Pearson, 2013.

