

Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>

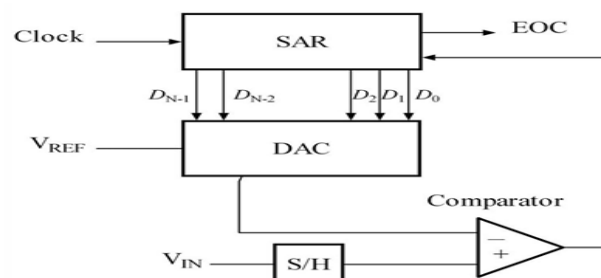
Name of the participant :Manwantha Krishnan

Title of the circuit :Design and Implementation of 8-bit Successive Approximation Register (SAR) ADC

Theory/Description :

A Successive Approximation Register (SAR) ADC is a type of analog-to-digital converter .It operates using a **binary search algorithm** to converge on the digital equivalent of an analog input voltage. The SAR ADC is widely used in data acquisition systems, embedded devices, and mixed-signal circuits because of its medium-to-high resolution (8–16 bits) and relatively fast conversion rates. The basic blocks of an 8-bit SAR ADC are:

1. **Sample and Hold Circuit** – captures the analog input voltage and holds it constant during conversion.
2. **Successive Approximation Register (SAR)** – a digital logic block that performs the binary search by successively setting and clearing bits from MSB to LSB.
3. **Digital-to-Analog Converter (DAC)** – generates an analog voltage corresponding to the current SAR output code.
4. **Comparator** – compares the DAC output with the input signal and provides feedback to the SAR logic.



Circuit Diagram(s):

Source/Reference(s) :

- 1)[Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs | Analog Devices](#)
- 2)[IJSPPR 8104 3129 https://www.ijspr.com/citations/v81n4/IJSPPR_8104_31293.pdf](https://www.ijspr.com/citations/v81n4/IJSPPR_8104_31293.pdf)