

Research Migration Project

Title: Design and Analysis of a StrongARM Latch Comparator Using eSIM

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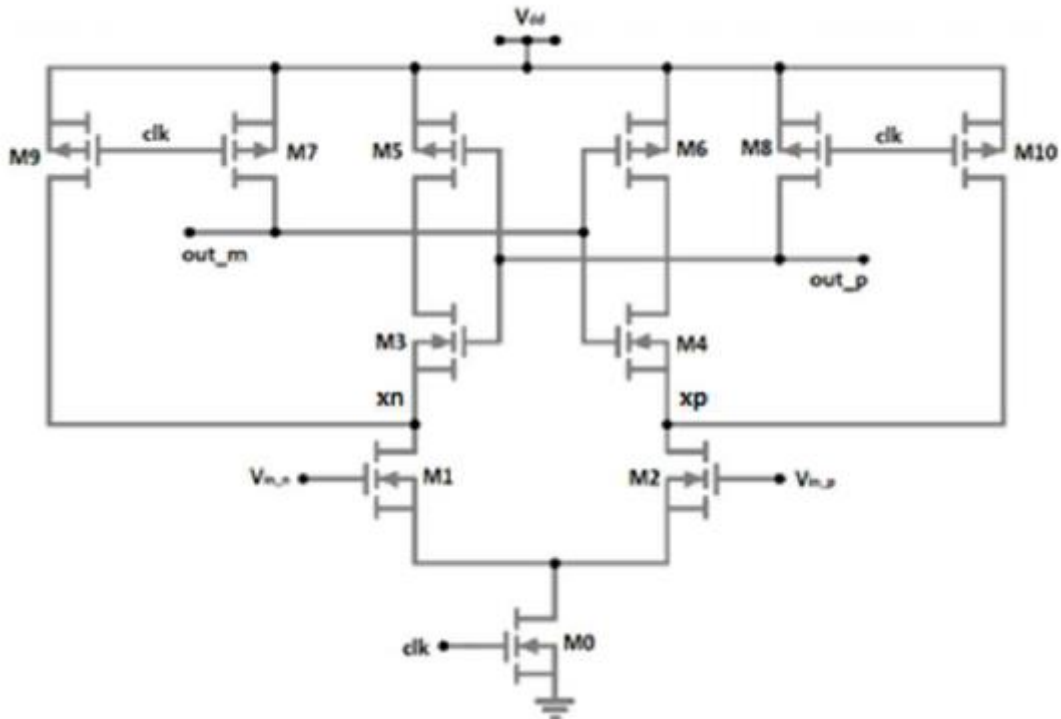
Introduction:

A comparator is an electronic circuit, often built with operational amplifiers, that compares two input signals and generates a corresponding output. A fundamental and advanced example is the Strong-Arm latch, a dynamic comparator designed for rapid and precise analog signal comparison. Key features like zero static power consumption, high input impedance, and a rail-to-rail output make it highly effective. Consequently, the Strong-Arm latch is widely integrated into circuits like Analog-to-Digital Converters (ADCs) and is critical for compact, energy-efficient electronics in modern applications such as IoT and wearable devices.

Objective:

- To study the operational principles of the StrongARM latch, i.e. reset and evaluation phases.
- To design the schematic of the complete comparator at the transistor level in eSIM.
- To perform transient analysis to verify its functionality and latching behaviour.

Circuit Diagram:



Expected output:

- A functional eSIM schematic and successful simulation of the StrongARM latch comparator.
- Waveform analysis demonstrating correct pre-charging and rapid rail-to-rail output generation during evaluation.

Reference:

P. Kishore, V. Tarun, S. R. V. S. Siva, and S. Kompella, "Design of Strong-Arm Latch Comparator for Low Power 12-bit SAR ADC," in *Proc. 2024 Int. Conf. Integr. Circuits Commun. Syst. (ICICACS)*, 2024.