1 Bit Full Adder Using CMOS Mirror Logic

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***Abstract*—This project presents the design and verification of a 1-bit Full Adder using CMOS mirror logic, which offers optimized performance in terms of area, power, and speed. The design leverages the fundamental properties of inversion and duality in CMOS logic to implement efficient logic gates with minimal transistor count. Mirror logic enables a symmetrical pull-up and pull-down network, reducing redundancy and improving switching characteristics. The circuit was modeled and simulated using eSim, an open-source EDA tool, and its functional correctness was verified through Ngspice transient analysis. The simulation results confirm accurate output for all binary input combinations, validating the use of CMOS mirror logic for compact and power-efficient arithmetic unit design in VLSI systems.**

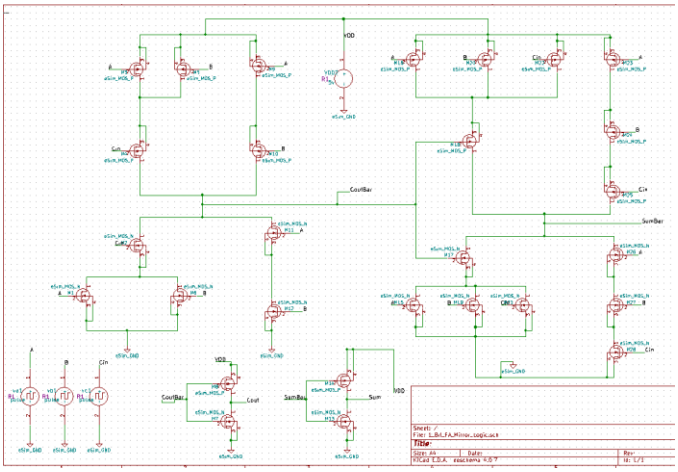
***Index Terms*—Duality , Inversion ,Transistor minimization , low power**

I. Introduction

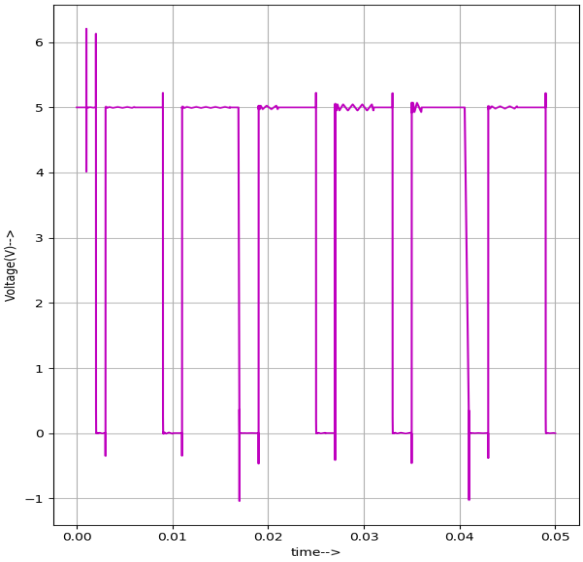
modern digital systems, arithmetic logic units (ALUs) play a pivotal role in executing computational tasks, and the full adder is a fundamental building block within these units. As the demand for compact, high-speed, and low-power integrated circuits increases, the design of efficient full adders becomes a critical focus area in VLSI research. Traditional CMOS logic styles, while functionally robust, often involve redundant transistors that can increase power consumption and area.

CMOS mirror logic emerges as a promising alternative due to its structural regularity and reduced transistor count. This logic style exploits the principles of duality and inversion, which allow the creation of complementary pull-up and pull-down networks in a mirror-symmetrical fashion. This mirroring not only simplifies the layout but also enhances performance by balancing delay paths and minimizing parasitic effects.

II. Implementation



III. Result



The waveform illustrates the SUM output of the 1-bit full adder implemented using CMOS mirror logic. Simulated in eSim with Ngspice, the output correctly transitions between logic levels (0 V and 5 V) for all eight input combinations of A, B, and Cin. The consistent and accurate transitions validate the correct functionality of the adder. Minor overshoots are present due to switching dynamics but do not affect logic integrity. Overall, the SUM output confirms the successful implementation of mirror logic for arithmetic operations.

IV. Conclusion

This research presented the design and analysis of a 1-bit full adder using CMOS mirror logic. The proposed design demonstrated reduced transistor count, improved symmetry, and reliable operation across all input states. The results validate the efficiency of mirror logic in optimizing area and power consumption, highlighting its suitability for scalable VLSI arithmetic units.

V. References

Dhanjal, I. S. (n.d.). Lecture Notes on VLSI Design [Class notes]. Department of Electronics