# Research Migration Project

National Institute of Technology Rourkela

**Name of the participant :** Krishnendu Roy

**Title of the circuit :** 2:1 Multiplexer Using Different Design Styles: Comparative Analysis

**Theory/Description :**

Multiplexers (MUX) are essential components in digital circuits, enabling efficient data selection and signal routing. This project focuses on the design and comparative analysis of a 2:1 multiplexer using different design styles, including conventional CMOS, Transmission Gate Logic (TGL), and Pass Transistor Logic (PTL).

Simulations are performed to analyze trade-offs between power efficiency and switching speed, providing insights into the advantages and limitations of each design style. The results demonstrate how different approaches impact circuit performance, making them suitable for various applications in low-power and high-speed digital systems. By comparing these methodologies, this study serves as a valuable reference for researchers and engineers working on optimized multiplexer designs in modern VLSI circuits.

**Circuit Diagram(s) :**

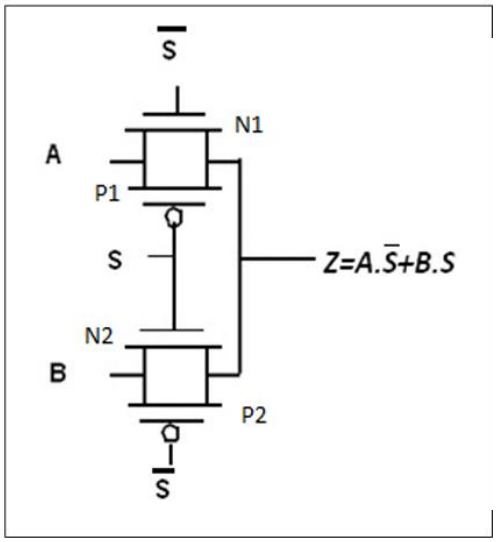


***Fig. 3:*** *2:1 MUX using transmission gate only.*

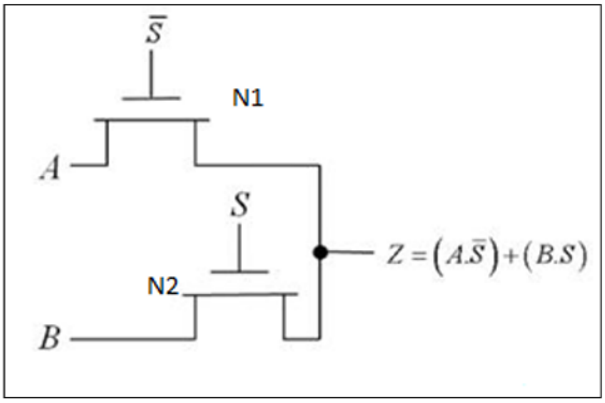


***Fig. 5:*** *Circuit diagram of 2:1 MUX using pass transistor only.*

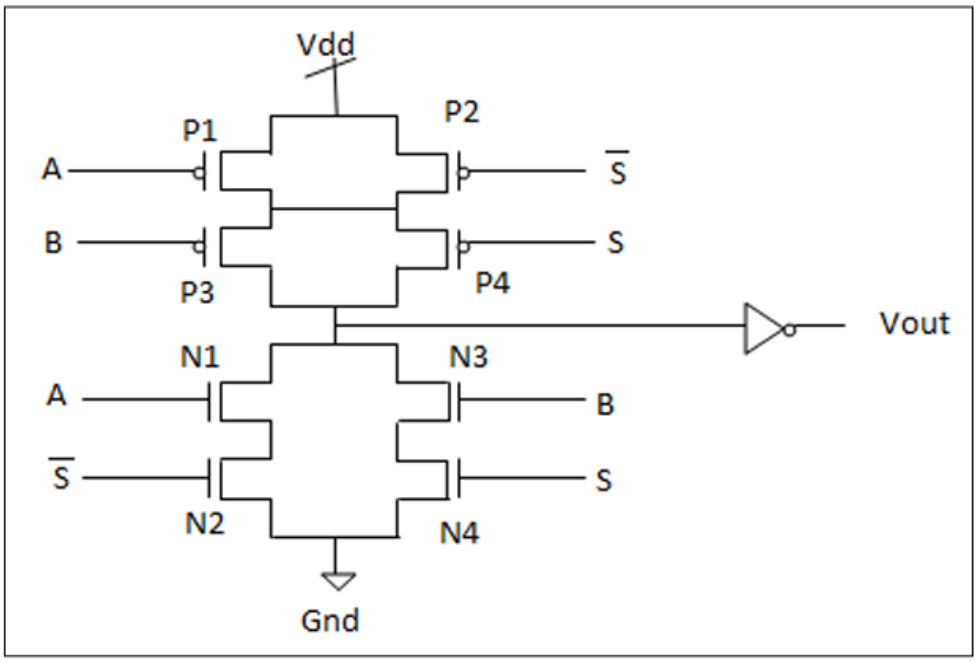


***Fig. 7:*** *2:1 MUX using CMOS logic only.*

**Source/Reference(s) :**

**Title of Paper:** 2:1 Multiplexer Using Different Design Styles: Comparative Analysis

**Link to paper:** (PDF) 2:1 Multiplexer Using Different Design Styles: Comparative Analysis