Research Migration Project

https://esim.fossee.in/research-migration-project

Name of the participant : **Sabarish Mohan JS**

Title of the circuit : **TR gate Based Design of Reversible Full Subtractor**

College : **Sri Sivasubramaniya Nadar College of Engineering, Chennai**

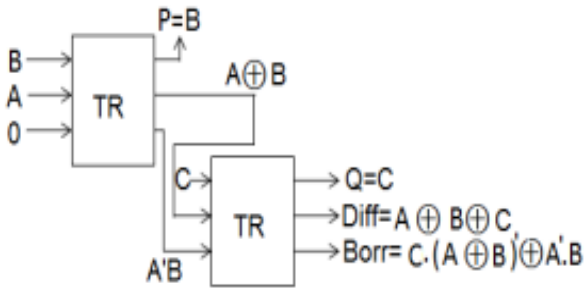
Problem Statement :

Design and simulation of a **reversible full subtractor using TR gates** in eSim to achieve low-power and information-preserving computation. The proposed design reduces energy dissipation, making it suitable for quantum computing, low-power VLSI, and fault-tolerant systems.

Description :

Reversible logic is a key technology for low-power computing, quantum circuits, and fault-tolerant digital systems, as it minimizes energy dissipation by preserving information. This project focuses on designing and simulating a reversible full subtractor using the TR gate, a reversible logic gate that ensures bijective mapping between inputs and outputs. The TR gate facilitates arithmetic operations while maintaining reversibility, making it a suitable building block for **power-efficient digital circuits**. The reversible full subtractor computes the difference and borrow outputs without energy loss, making it highly applicable in quantum computing, cryptographic hardware, and low-power VLSI designs. Implemented in eSim, an open-source EDA tool, the proposed design enables efficient arithmetic operations with minimal power dissipation. Its potential applications include low-power processors, error-resilient digital systems, and emerging nanotechnology-based computing architectures.

Circuit Diagram(s) :



Proposed TR gate Based Design of Reversible Full Subtractor

Truth table of full subtractor:

A	B	C		Borr	Diff
0	0	0		0	0
0	0	1		1	1
0	1	0		1	1
0	1	1		1	0
1	0	0		0	1
1	0	1		0	0
1	1	0		0	0
1	1	1		1	1

Source :

1.TITLE : Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate

AUTHOR : Himanshu Thapliyal and Nagarajan Ranganathan

LINK : https://ieeexplore.ieee.org/abstract/document/5076412?casa_token=Ge44z1H7nxcAAAAA:rU2p96NTJqQrF2wPA38Jzi9k-dvWzy826Oq9Iy_K5TT6RJvuNlEsOkWSCyc-PvHLc1hk5kQ6N4PW

2. TITLE : Design and Implementation of an Efficient Reversible Comparator Using TR Gate

AUTHOR : Subramanian Saravanan1, Ila Vennila1, Sudha Mohanram

LINK : https://www.scirp.org/journal/paperinformation?paperid=69136