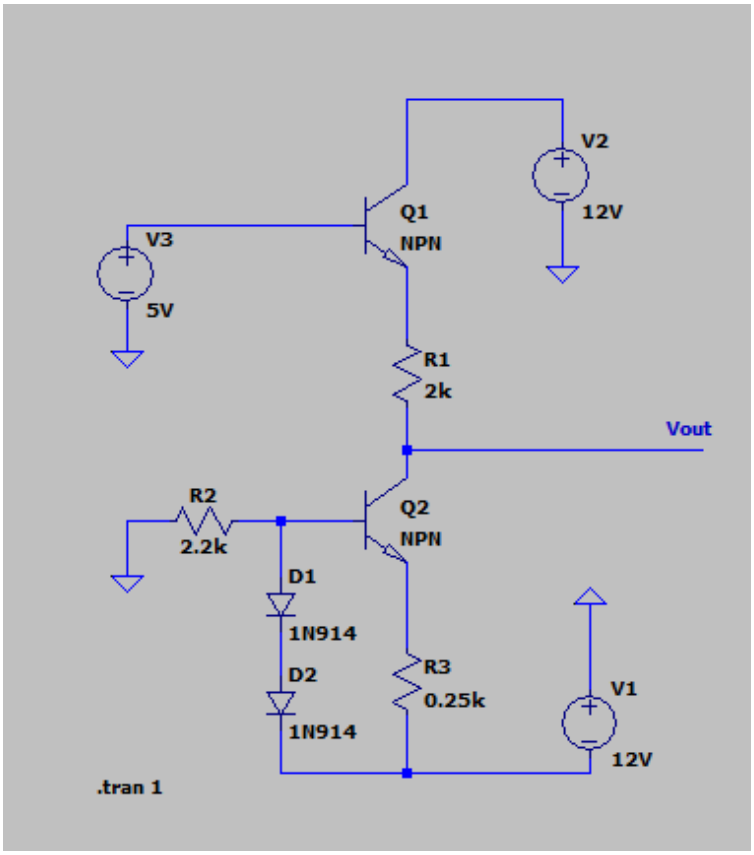
Daul BJT Voltage Level Shifter Circuit

Problem Statement:

Design a level shifter using NPN BJT to remove DC from the circuit. If the DC is present in the circuit it may leads attenuation of signals in amplifer and reduces power dissipation in complex circuits .And In System-on-Chip (SoC) design, different components like digital circuits, analog blocks, and passive elements are integrated on a single chip. These components often require different operating voltages to function efficiently and achieve optimal performance. To allow communication between these different voltage domains, a **level shifter cell** is used it converts signal voltages from one domain to another within the VLSI system. One effective way to reduce both leakage and dynamic power in such systems is by using multiple power supplies. This approach becomes especially important when a chip interfaces between core circuits and input/output circuits. Without proper voltage translation, a signal from one domain might not be correctly recognized by another due to mismatched voltage ranges, potentially leading to unreliable behavior or even circuit failure. Level shifters solve this issue by ensuring safe and accurate signal transfer across varying voltage levels.

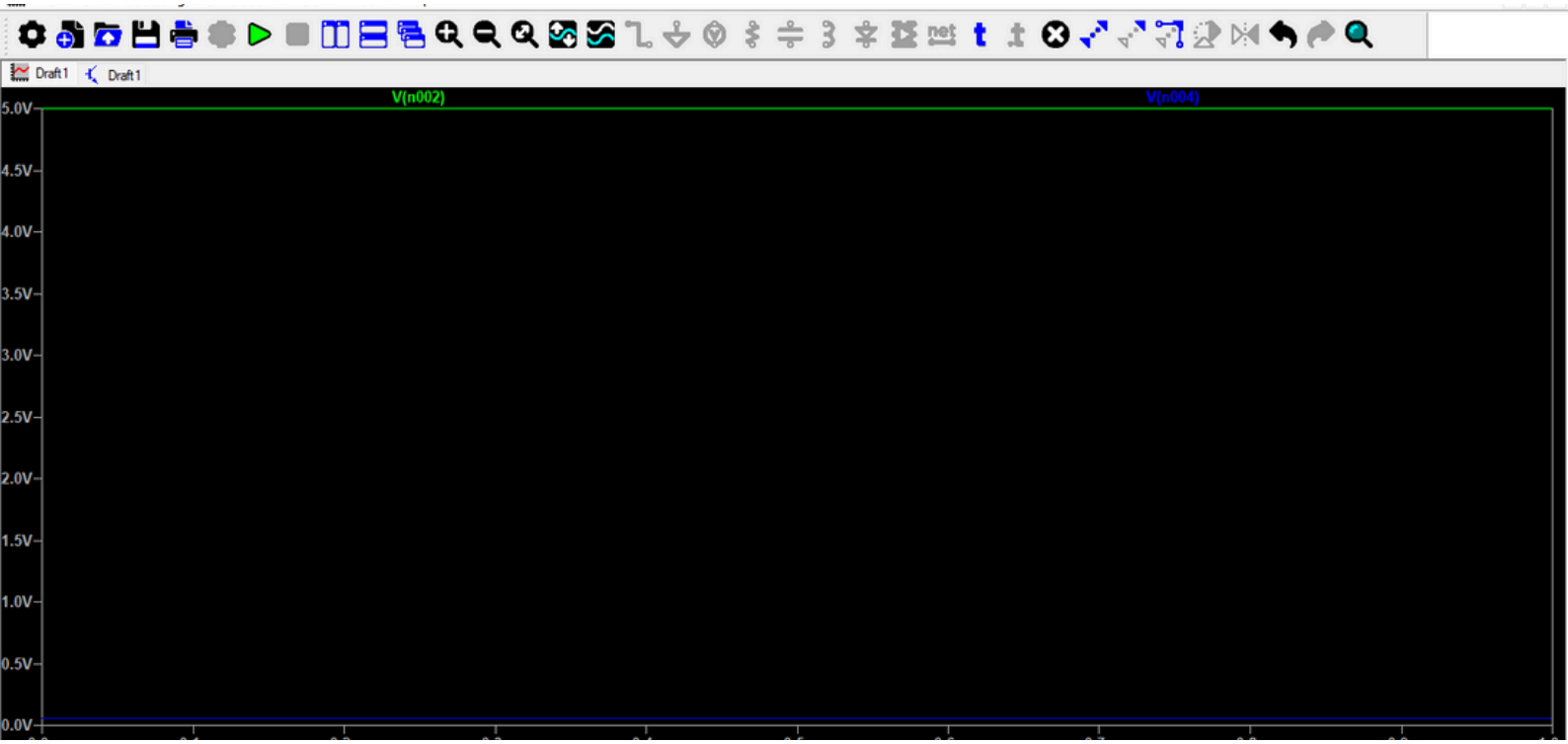
Solution:

Design Overview:



Level Shifter Using Dual BJT

Design Simulations:



The following image shows the response of Level shifter Circuit reducing DC 5V to DC 0.8 V

INPUT: 5V -------> OUTPUT :0.8V

References:

1. https://ieeexplore.ieee.org/document/7570905
2. Behzad Razavi, (2001) “Design of Analog CMOS Integrated Circuits”, Newyork: McGraw-Hill, 2nd edition.