LAHAF: Low-power, area-efficient, and high-performance approximate full adder based on static CMOS Implementation Using eSim

Name of the Participant: KARTHIKEYAN S

Institute: Loyola ICAM College of Engineering and Technology (LICET)

University: Anna University

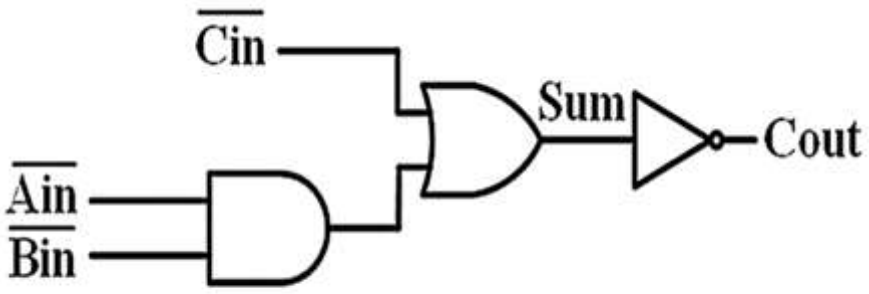
Problem Statement:

Exact adders provide high accuracy but consume significant power. Complex applications such as image processing, machine learning, and data mining can benefit from approximate computing techniques. Due to the limitations of human visual perception, approximate computing can be effectively applied to image and video processing applications.

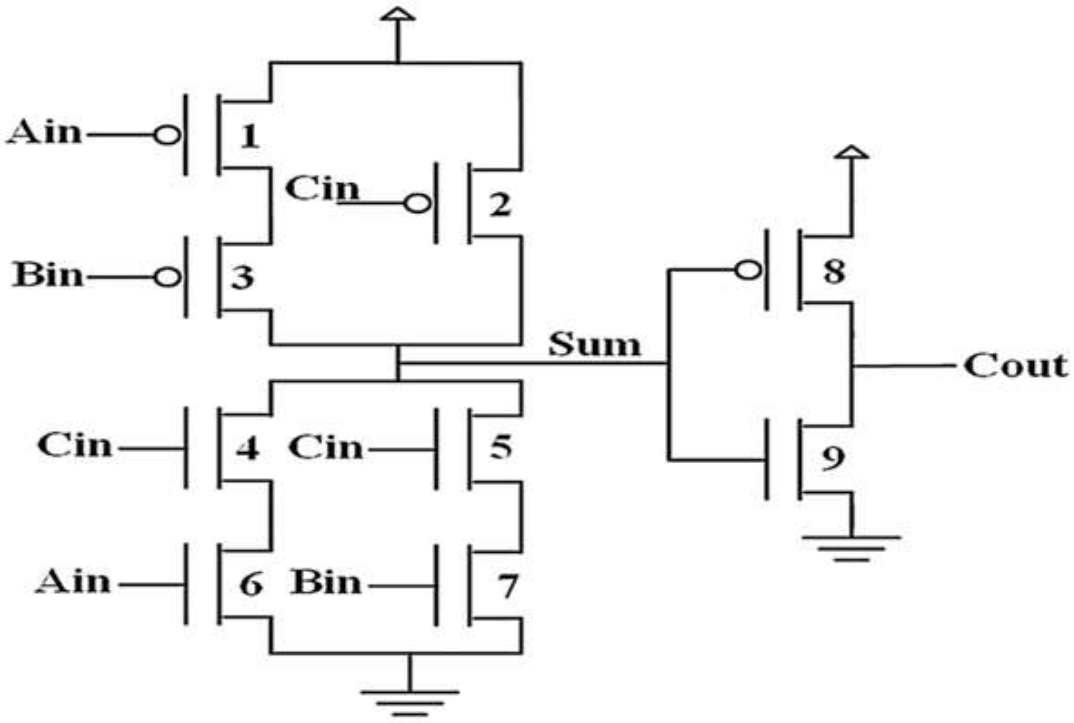
Description:

Designing an approximate full adder enables the evaluation of power consumption, propagation delay, and circuit efficiency. Implementing this adder within larger structures, such as a 4-bit Ripple Carry Adder or Carry Save Adder, allows for assessing the overall efficiency of the system. Approximate adders can enhance performance while reducing power consumption to attain low power. Image and video processing applications within DSP blocks can leverage error-tolerant designs for improved efficiency. Error analysis can be conducted using metrics such as Error Distance (ED) and Error Rate (ER) to quantify the trade-offs between accuracy and performance.

Circuit Diagram:



(a) Gate-level



(b) Transistor-level

Reference:LAHAF: Seyed Erfan Fatemieh, Samira Shirinabadi Farahani, Mohammad Reza Reshadinezhad “Low-power, area-efficient, and high-performance approximate full adder based on static CMOS”.Sustainable Computing: Informatics and Systems Volume 30, June 2021.

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