

Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>

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Title of the circuit: Design and analysis of TTL inverter

Theory/Description: A standard ttl circuit for an inverter in whicg q1 is the input coupling transistor, and d1 is the input clamp diode. Transistor q2 is called a phase splitter, and the combination of q3 and q4 forms the output circuit often referred to as a totem-pole arrangement. When the input is a high, the base-emitter junction of q1 is reverse-biased, and the base-collector junction is forward-biased. This condition permits current through r1 and the base-collector junction of q1 into the base of q2, thus driving q2 into saturation. As a result, q3 is turned on by q2, and its collector voltage, which is the output, is near ground potential. Therefore, there is a low output for a high input. At the same time, the collector of q2 is at a sufficiently low voltage level to keep q4 off. When the input is low, the base-emitter junction of q1 is forward-biased, and the base-collector junction is reverse-biased. There is current through r1 and the base-emitter junction of q1 to the low input. A low provides a path to ground for the current. There is no current into the base of q2, so it is off. The collector of q2 is high, thus turning q4 on. A saturated q4 provides a low-resistance path from vcc to the output; therefore, there is a high on the output for a low on the input. At the same time, the emitter of q2 is at ground potential, keeping q3 off. Diode d1 in the ttl circuit prevents negative spikes of voltage on the input from damaging q1. Diode d2 ensures that q4 will turn off when q2 is on (high input). In this condition, the collector voltage of q2 is equal to the base-to-emitter voltage, v_{be} , of q3 plus the collector-to-emitter voltage, v_{ce} , of q2. Diode d2 provides an additional v_{be} equivalent drop in series with the base-emitter junction of q4 to ensure its turn-off when q2 is on.

Circuit Diagram(s):

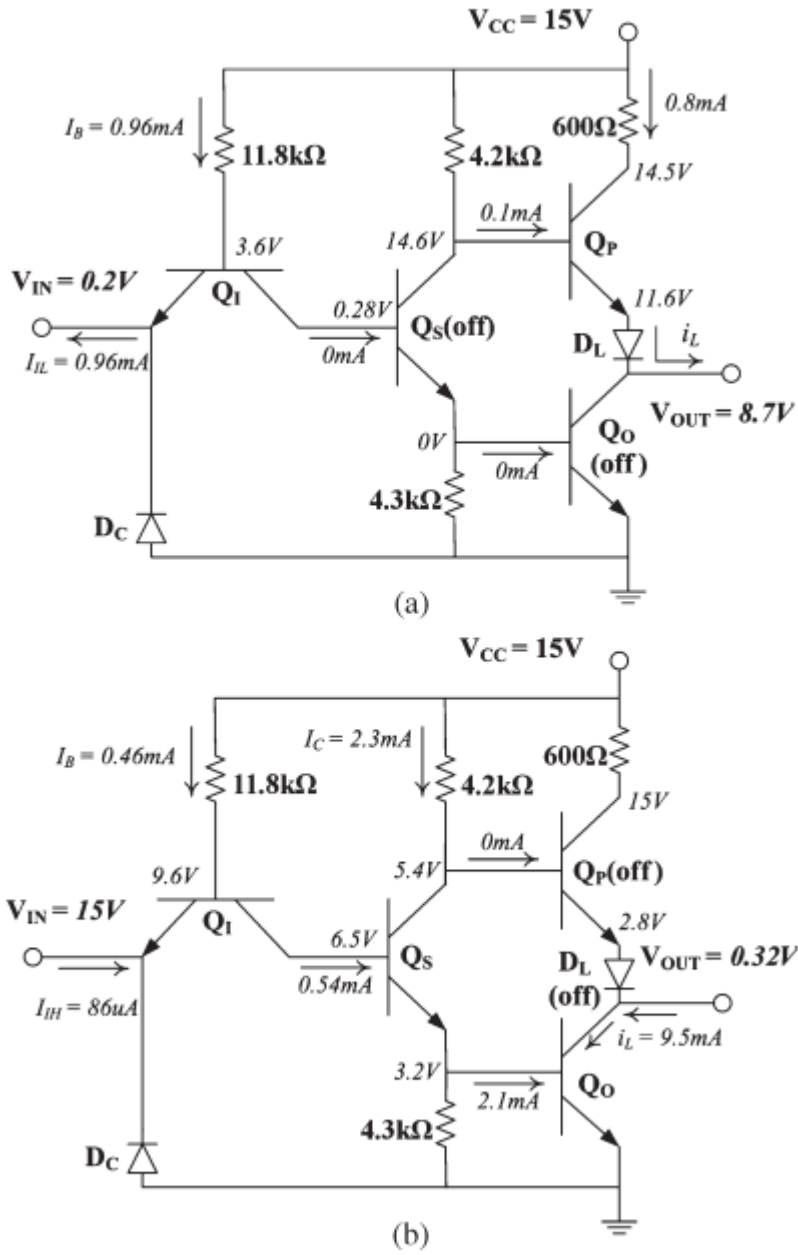


Fig. 2. Circuit diagram of the SiC TTL inverter implemented in this paper. Internal currents and voltages are shown for the inverter with a fan-out of ten in (a) the output-high state and (b) the output-low state.

Results (Input, Output waveforms and/or Multimeter readings):

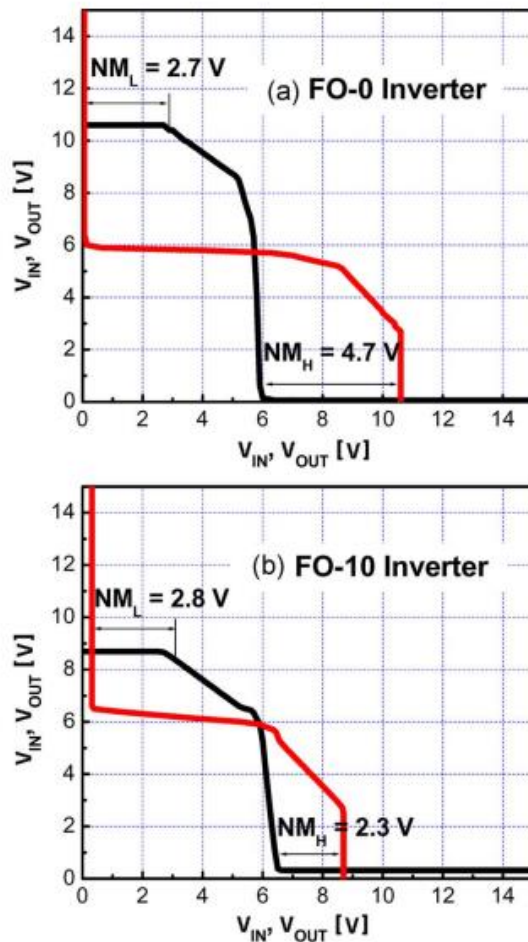


Fig. 3. SPICE simulations of the $V_{OUT}-V_{IN}$ characteristics for the SiC TTL inverter with $V_{CC} = 15$ V, $L = 100$ μm , and $L(Q_O) = 500$ μm at fan-outs of zero and ten. Static noise margins are also indicated.

Source/Reference(s):

- Demonstration and Characterization of Bipolar Monolithic Integrated Circuits in 4H-SiC Jeong-Youb Lee, Shakti Singh, and James A. Cooper, Fellow, IEEE
Article in IEEE Transactions on Electron Devices · September 2008 DOI: 10.1109/TED.2008.926681 · Source: IEEE Xplore.
- Digital Fundamentals by Thomas L. Floyd.