Title : Design and Implementation of 2*4 decoder and 3*8 decoder using 2*4 decoders in eSim

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Problem Statement : To design and implement a 2×4 Decoder and a 3×8 Decoder using 2×4 Decoders in eSim. Evaluate their performance based on logical complexity, power consumption, and efficiency. Apply modular design principles to construct the larger decoder using smaller components for optimal resource utilization.

Abstract : Decoders are integral components in digital systems, widely applied in memory addressing, data routing, and logic function implementation. This project aims to design and simulate a 2×4 Decoder using basic logic gates and then extend its application by constructing a 3×8 Decoder using multiple 2×4 Decoders through an efficient modular design approach. By employing eSim, an open-source electronic design automation (EDA) tool, the design will be analyzed for its performance and correctness.

The study will compare the implementation's effectiveness by evaluating power consumption, latency, and logical complexity. The use of hierarchical design enables the efficient construction of larger decoders from smaller units, which is particularly advantageous for digital systems requiring scalable and reusable components. The results will validate the feasibility and efficiency of the design, offering insights for further optimization in digital circuit design.

Proposed Circuit :

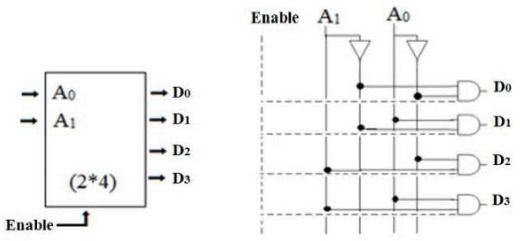

Figure 1: The block diagram and internal circuit of 2*4 decoder

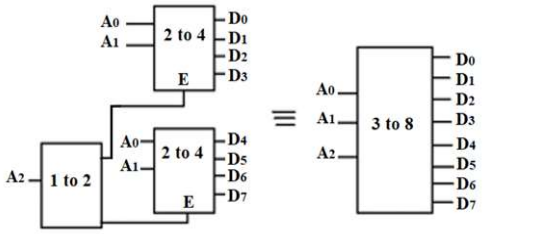

Figure 2: Building a 3*8 decoder using a group of 2*4 decoders.

Reference paper link :
Designing and Analyzing Decoders for Optimal Efficiency in Digital Systems, Leads to a Comparative Review