TITLE: **Design and Verification of Low Power SRAM using 8T SRAM Cell Approach**

STUDENT NAME: Athish I.S

COLLEGE: National Institute of Technology, Tiruchirappalli

PROBLEM STATEMENT:

SRAM (Static Random-Access Memory) is a key component in modern processors and portable devices, mainly used for on-chip cache memory. However, the traditional 6T SRAM design has issues with read stability and power consumption, making it less reliable for low-power applications.

Challenges:

1. Stability Issues in 6T SRAM – During read operations, noise can cause data flipping, leading to errors.
2. High Power Consumption – Existing 8T SRAM designs improve stability but suffer from bitline leakage, wasting energy.
3. Technology Scaling Effects – As transistors become smaller (45nm and below), variations in device properties affect SRAM performance.

OBJECTIVE:

This research proposes a modified 8T SRAM cell that improves Read SNM, reduces power consumption, and minimizes bitline leakage. The proposed design is implemented in 45nm CMOS technology, demonstrating superior stability and efficiency compared to existing 6T and 8T SRAM architectures

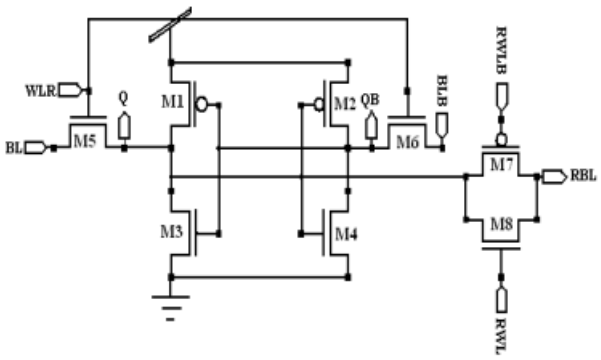

Fig 8: Proposed 8T SRAM Cell

REFERENCES:

https://research.ijcaonline.org/volume67/number18/pxc3887201.pdf