Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant : Krishnendu Roy

Title of the circuit : Design, Simulation, and Investigation of Basic Logic Gates by Using NAND Logic Gate

Theory/Description :

The NAND logic gate is one of the universal logic gates. We can use it to design and build a digital logic gate like (not, and, or) gates. This paper gives Design, Simulation, and Investigation of Basic gates by utilizing NAND Gate with perfect output logic standards with preserving similar performance for all digital logic in this design, we can use it easily to create very large-scale integration (VLSI)designing. In our simulation has been tested on the hspice program at 32 nm CMOS technology. The results show this design has low lower dissipation and delay when compared with other designs. When compared to some of these designs, the findings reveal that the intended gate is typically quicker, shorter, and with much less energy dissipation, and there's a boom in pace and electricity dissipation for the reason that processing era improves 32nm. In addition, the recommended 4T became proven to be quicker than others. In evaluation to the standard CMOS NAND gate, which employs a few transistors, the recommended layout has furnished a sparkling new shape for developing a enter NAND gate making use of simply 4 transistors. The suggested design gate can predict the creation of devices with significantly improved speed, energy consumption, and computationally efficiency.

Circuit Diagram(s) :

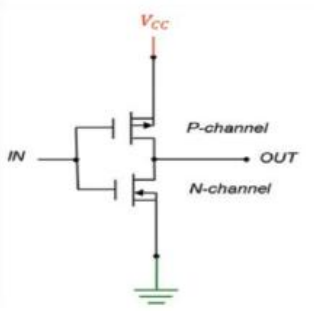
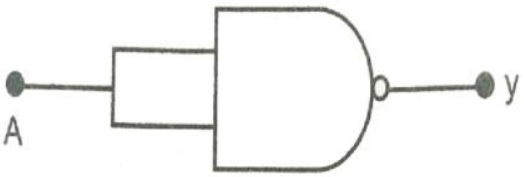


FIGURE 1. Not circuit



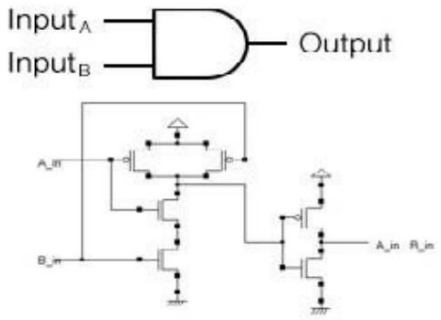


FIGURE 3. AND gate cricuit

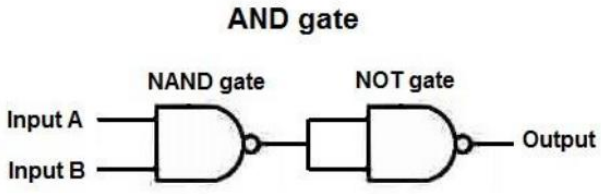
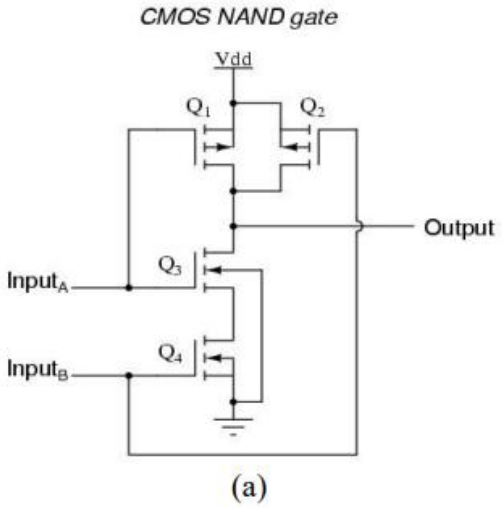
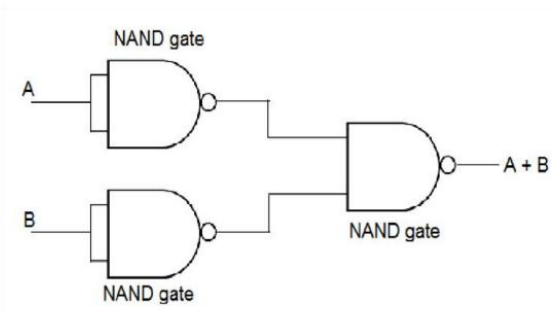


FIGURE 7. AND logic gate



(a)



Results (Input, Output waveforms and/or Multimeter readings) :

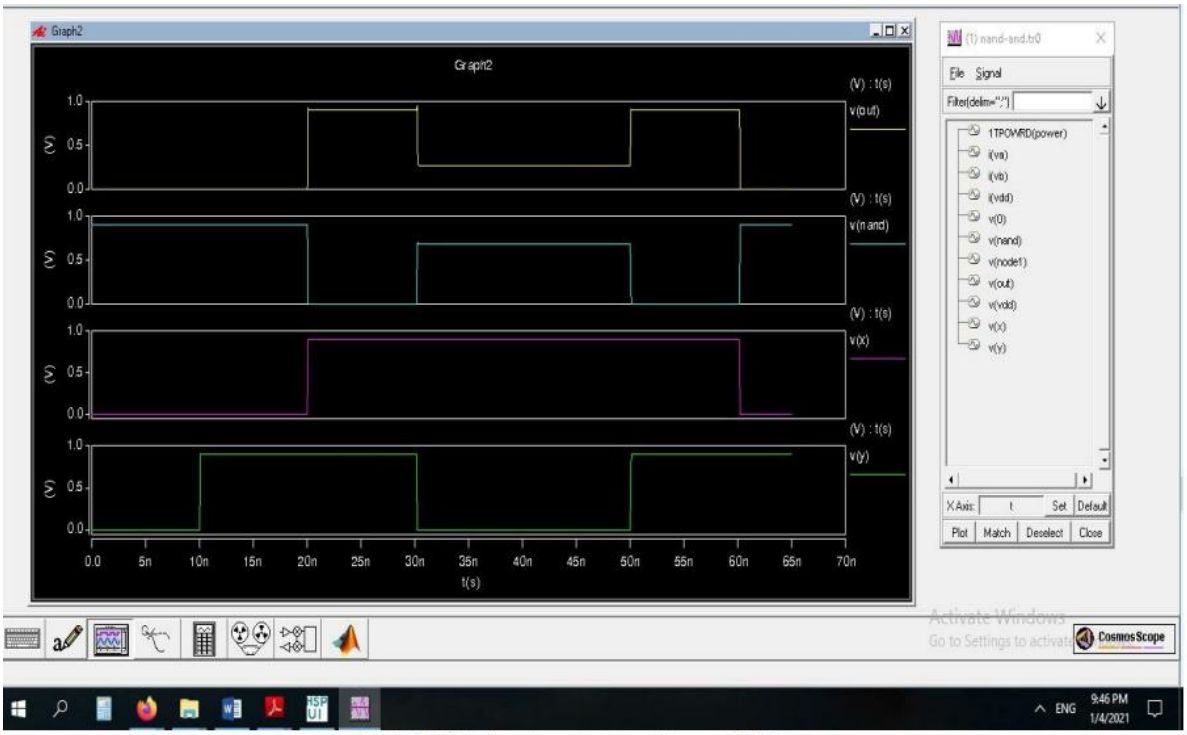
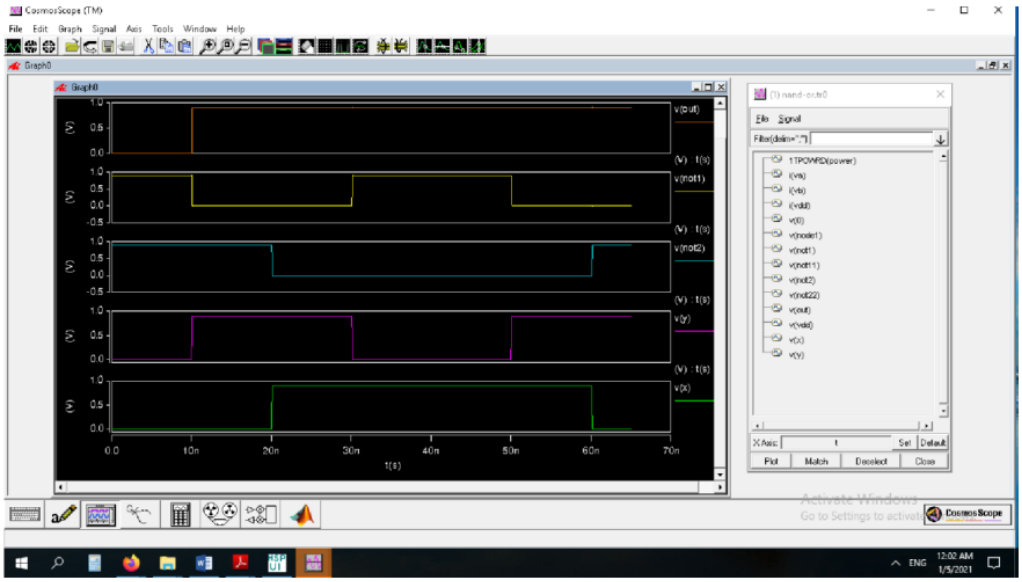


FIGURE 8. input-output waveforms AND gate

FIGURE 9. OR logic gate



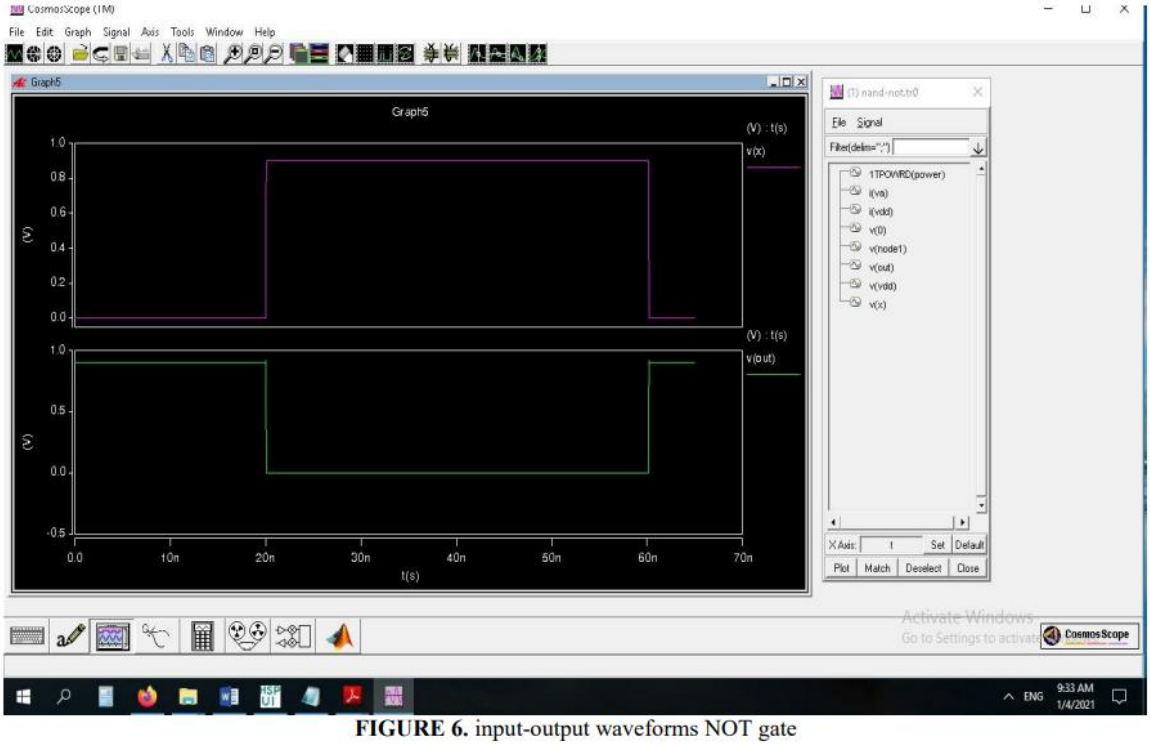


FIGURE 6. input-output waveforms NOT gate

Source/Reference(s) :

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Link to paper: (PDF) Design, simulation, and investigation of basic logic gates by using NAND logic gate