Design of a 5x5 Wallace Tree Multiplier

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Abstract

A Central Processing Unit allots majority of its processing time to arithmetic operations. Almost every signal processor today has a set of dedicated multiplier units. Multiplication requires more hardware and execution time as compared to addition or subtraction process. Thus a need of high speed multipliers arises. Wallace Tree Multiplier is one such method of multiplication which uses carry save algorithm to reduce the computational time. In this architecture, all the bits of the partial product are added in parallel without propagating the carry's thus increasing speed. This process is repeated until two rows are left which are added by carry propagate adder.

Algorithm of Reference Circuit

The pictorial representation explaining the working of 5x5 Wallace Tree Multiplier is as shown in fig 1.

- The method first generates a set of partial products obtained by multiplying each number bit by bit.
- These partial products are added parallelly using half adder and full adder resulting in two outputs, sum and carry.
- This method continues until two rows are left which when added produces the final result.

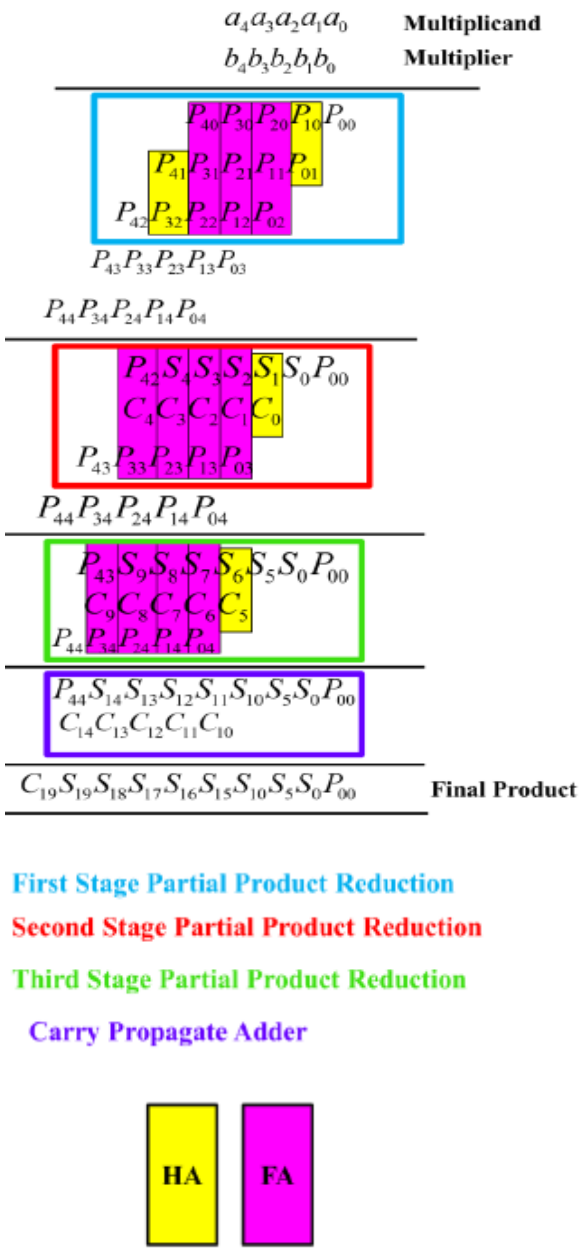

Fig 1: Algorithm of Wallace Tree Multiplier.

Details of Reference Circuit

The Schematic of the 5x5 Wallace Tree Multiplier is shown on fig 2.

Each of the 5-bit Multiplier and Multiplicand when multiplied result in a 10-bit product. This can be implemented using Half Adder, Full Adder and AND Gates as shown.

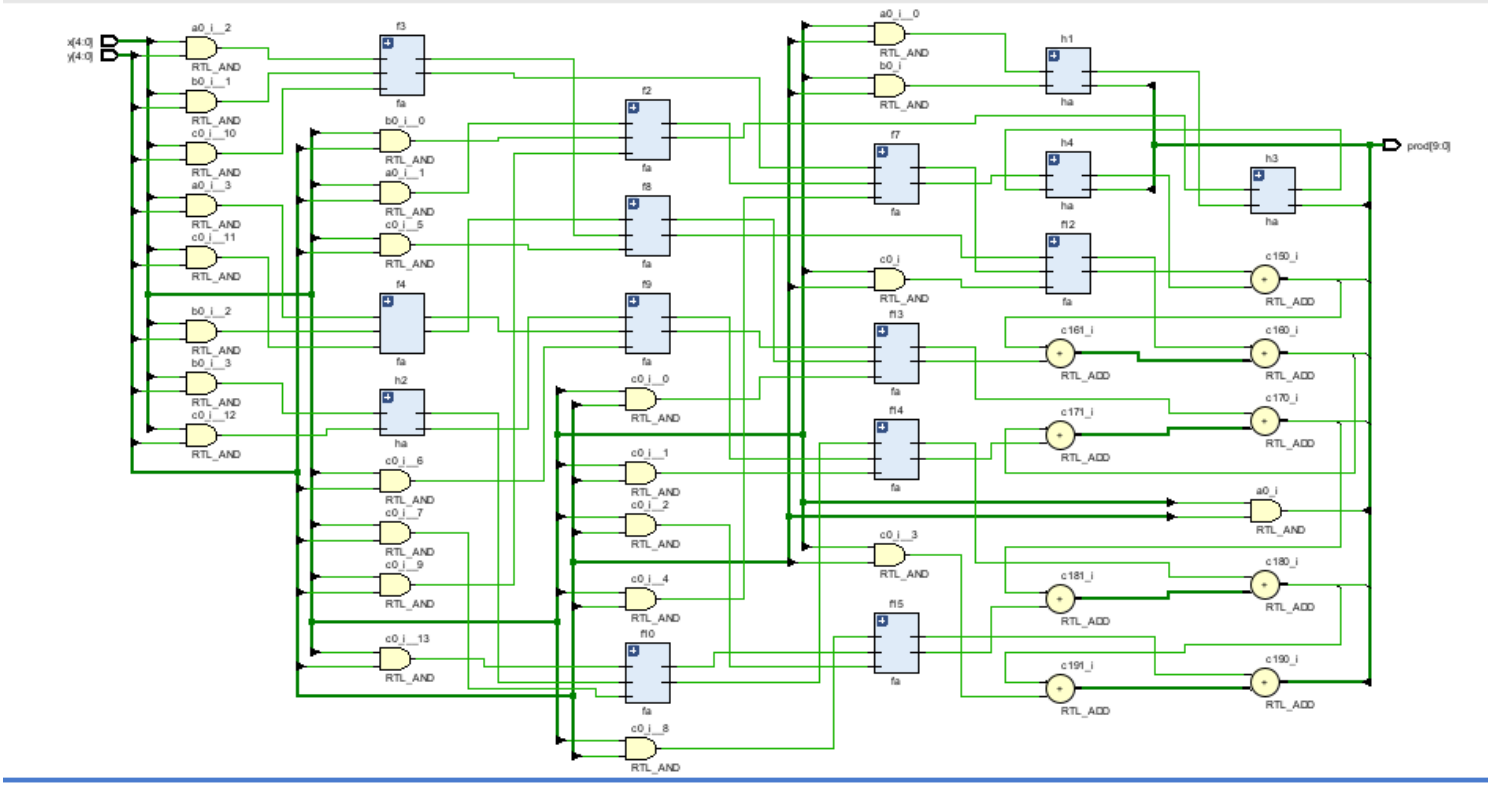

Fig 2: Schematic of 5x5 Wallace Tree Multiplier.

Waveforms of Reference Circuit

The Waveforms of the 5x5 Wallace Tree Multiplier is shown on fig 3.

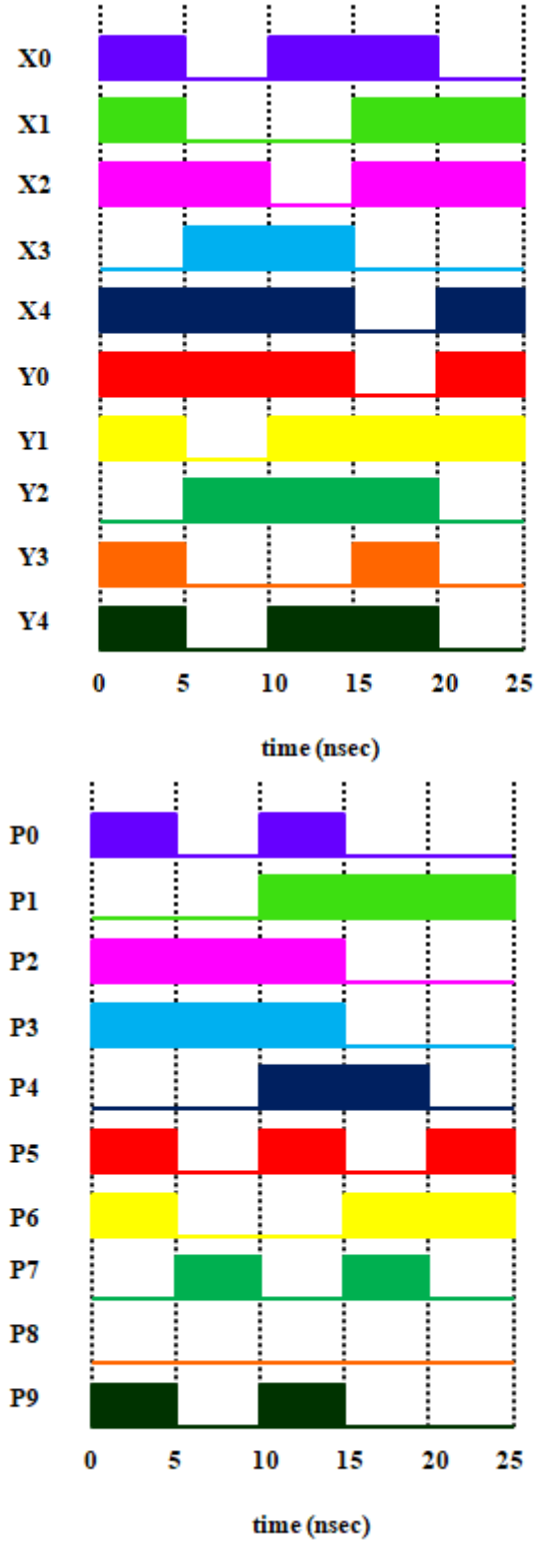

Fig 3: Waveforms of 5x5 Wallace Tree Multiplier.

References

[1] Youtube Video - https://www.youtube.com/watch?v=lcPIMvI57dM&t=114s

[2] Comparison of Vedic Multiplier with Conventional Array and Wallace Tree Multiplier by ANU THOMAS, ASHLY JACOB, SERIN SHIBU, SWATHI SUDHAKARAN.