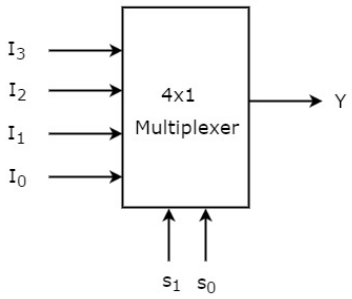
MIXED CIRCUIT IN 4:1 MULTIPLEXER USING ESIM

Susmitha T – Bannari Amman Institute of Technology, Erode

Abstract- A multiplexer is a unidirectional device that is utilized in any application where data must be switched from numerous sources to a destination. Modern VLSI design now places a high premium on low power circuits. Here we are implementing the 4:1 multiplexer using eSim simulator. Digital and Analog circuits of a certain circuit are both included in mixed signal circuits. A data selector called MUX produces a single output from several data inputs. Here, we've put into practice a two-input MUX that will produce a single output depending on a single line of input.

1. DESCRIPTION:

A multiplexer is a combinational circuit that has a single output line, n selection lines, and up to 2n data inputs. On the basis of the values of the selection lines, one of these data inputs will be connected to the output. There will be 2n potential combinations of zeros and ones as there are 'n' selection lines. Thus, just one data input will be chosen for each combination. Another name for a multiplexer is a Mux. A 4-to-1 multiplexer has a single output line (Y), two select lines (S0 and S1), and four data input lines (D0 to D3). The four input lines are chosen by the select lines S0 and S1 to link to the output line.



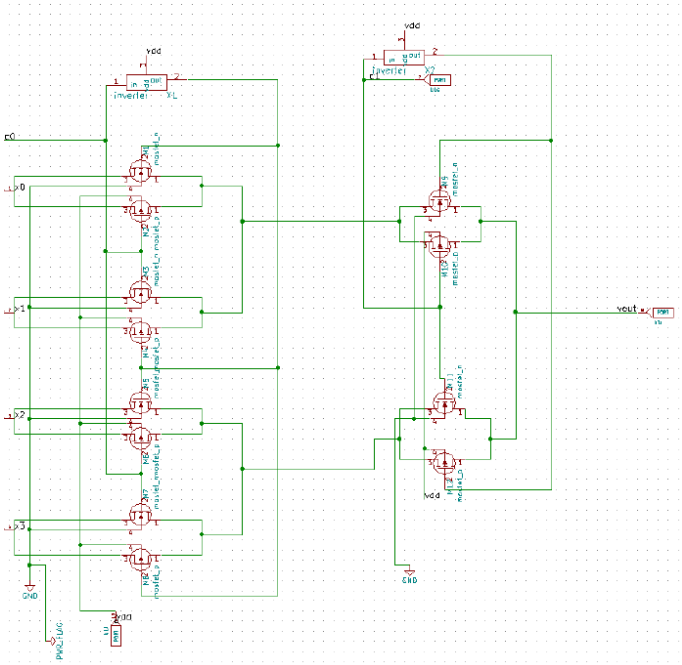
The input line that will be chosen to pass from the multiplexer will be D0 when selection lines A and B both have values of 0. As a result, for input line D0, MUX will short circuit, and for all other input lines, it will be open circuited.

The input line that will be chosen is D1 if selection line A represents 0 and selection line B represents 1. In this scenario, MUX will act as an open circuit for all other input lines while acting as a short circuit for input line D1.

The output will produce the input line D2 if the selection line A is 1 and the selection line B is 0. In this case, the MUX will only let D2 travel through it and will block all other input.

The last input line, D3, will be chosen if both selection lines have the value 1. In this scenario, the MUX will only permit the D3 to flow through it, preventing the passage of other input lines.

2. IMPLEMENTED DIAGRAM



3. REFERENCE

(1) Performance Evaluation of 4:1 multiplexer - https://iaeme.com/MasterAdmin/Journal_uploads/IJECET/VOLUME_7_ISSUE_4/IJECET_07_04_003.pdf

(2) High performance, low power 200 Gb/s 4:1 MUX with TGL in 45 nm technology - https://link.springer.com/article/10.1007/s13204-013-0206-0