

Design of 4-Bit Pipelined Vedic Multiplier using Kogge Stone PPA using eSim and SKY130

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Abstract—The multiplier is a key building block of all processors, which improves the speed of Digital Signal Processor (DSP), a special application in which we need to reduce the time delay. In the proposed method, we design a Vedic multiplier by using a Vedic Mathematics Sutra called Urdhva Tiryagbhyam. The same basic concept is extended to the multiplication of binary numbers to make use in the digital hardware system. This vedic multiplier can be used in many fast computing processors because of their less time delay and less hardware area.

I. INTRODUCTION

Urdhva Tiryagbhyam sutra which is the general formula applicable to all cases of multiplication. Urdhva means “Vertically” and Tiryagbhyam means “Crosswise”.

II. BASIC ALGORITHM OF VEDIC MULTIPLIER

These are the following steps followed in this process.

Step-1: Units place digits are multiplied.

Step-2: Cross multiplication (units place of 1st number is multiplied with tens place of 2nd and vice versa and then both are added) and add the carry from Step-1.

Step-3: Tens place digits are multiplied and add carry from Step-2.

Pictorial format of these steps are shown in Fig. 1.

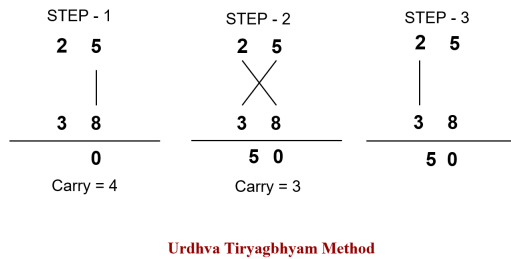


Fig. 1. Decimal Multiplication Example

The above method is also followed when we have to deal with binary numbers. But instead of directly taking the binary digits we club multiple digits (here it is 2) into a set and follow the method on the set. In the following example 1110 (14) is multiplied with 1001 (9). 1110 is divided into 2 sets as 11 10 and similarly 1001 to 10 01. Pictorial format of these steps are shown in Fig. 2.

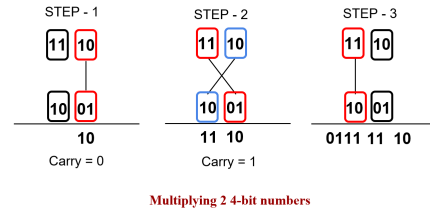


Fig. 2. Binary Multiplication Example

III. PIPELINED VEDIC MULTIPLIER ARCHITECTURE

Block diagram of the 4-bit Pipelined Vedic Multiplier can be shown in Fig. 3. The overall design has 2 parts i.e. one before the 16-bit DFF is a **Partial Product Generator** and the one after 16-bit DFF along with 16-bit DFF is the **Final Product Generator** from partial products. For the combinational design we can just ignore the 16-bit DFF and connect the partial products directly to the final product generator part.

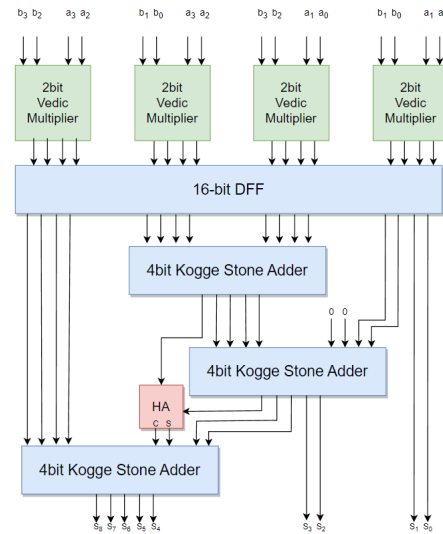


Fig. 3. Block Diagram of 4-bit Pipelined Vedic Multiplier with KSA PPA

REFERENCES

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- [2] T. Sutra, "Design of Vedic multiplier using Urdhva Tiryagbhyam Sutra" <https://www.semanticscholar.org/paper/Design-of-Vedic-multiplier-using-Urdhva-Tiryagbhyam-Sutra/29e50274fddab42ec935af57a39aac92080c9e6c>