

Design of 4-Bit Pipelined Vedic Multiplier using Kogge Stone PPA using eSim and SKY130

Ch Kalyan Kumar Prusty
Bangalore, India
kalyanprusty@gmail.com

Abstract—The multiplier is a key building block of all processors, which improves the speed of Digital Signal Processor (DSP), a special application in which we need to reduce the time delay. In the proposed method, we design a Vedic multiplier by using a Vedic Mathematics Sutra called Urdhva Tiryagbhyam. The same basic concept is extended to the multiplication of binary numbers to make use in the digital hardware system. This vedic multiplier can be used in many fast computing processors because of their less time delay and less hardware area.

I. INTRODUCTION

Urdhva Tiryagbhyam sutra which is the general formula applicable to all cases of multiplication. “**Urdhva**” and “**Tiryagbhyam**” words are derived from Sanskrit literature. Urdhva means “**Vertically**” and Tiryagbhyam means “**Crosswise**”. It is based on a novel concept, where the generation of all intermediates can be done with the concurrent addition of partial products.

II. BASIC ALGORITHM OF VEDIC MULTIPLIER

These are the following steps followed in this process.

Step-1: Units place digits are multiplied.

Step-2: Cross multiplication (units place of 1st number is multiplied with tens place of 2nd and vice versa and then both are added) and add the carry from Step-1.

Step-3: Tens place digits are multiplied and add carry from Step-2.

Pictorial format of these steps are shown in Fig. 1.

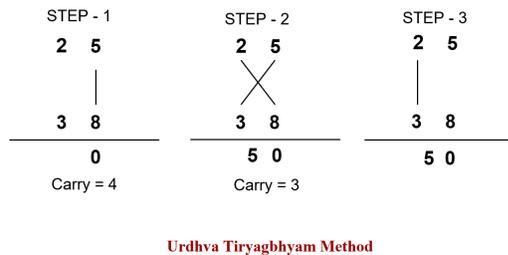


Fig. 1. Decimal Multiplication Example

The above method is also followed when we have to deal with binary numbers. But instead of directly taking the binary digits we club multiple digits (here it is 2) into a set and follow the Urdhva Tiryagbhyam method on the set. In the following example 1110 (14) is multiplied with 1001 (9). 1110 is divided into 2 sets as 11 10 and similarly 1001 to 10 01. Pictorial format of these steps are shown in Fig. 2.

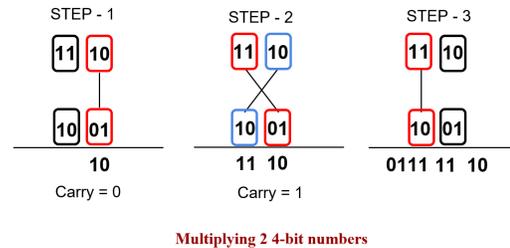


Fig. 2. Binary Multiplication Example

III. PIPELINED VEDIC MULTIPLIER ARCHITECTURE

Block diagram of the 4-bit Pipelined Vedic Multiplier can be shown in Fig. 3. The overall design has 2 parts i.e. one before the 16-bit DFF is a **Partial Product Generator** which is a complete analog design designed in eSim, is simulated with **NgSpice SKY130** library and the one after 16-bit DFF along with 16-bit DFF is the **Final Product Generator** from partial products which is a completely digital, designed using **Verilog HDL** is simulated verified in **Makerchip**. For the combinational design we can just ignore the 16-bit DFF and connect the partial products directly to the final product generator part.

A. Analog Designing Part

For designing the multiplier we start with the basic gates required for the design i.e. **NOT**, **AND**, **XOR**. The schematic for the same is shown in Fig. 4, Fig. 5 and Fig. 6 respectively.

Using the AND gate and XOR gate Half Adder is designed which is shown in Fig. 7.

Here for all the basic gates the overall W/L ratio of PMOS to overall W/L ratio of NMOS is maintained 2 (assuming mobility_{of_electron}/mobility_{of_hole} = 2) such that the rise time and fall time will be same. Hence while designing these gate the maintained W/L ratio is shown in following table.

Gate name	PMOS or NMOS	(W/L) ratio
NOT	SC1 (PMOS)	2
NOT	SC2 (NMOS)	1
AND	SC1,SC4 (PMOS)	2
AND	SC2,SC3 (NMOS)	2
XOR	SC1,SC2,SC5,SC6 (PMOS)	4
XOR	SC3,SC4,SC7,SC8 (NMOS)	2

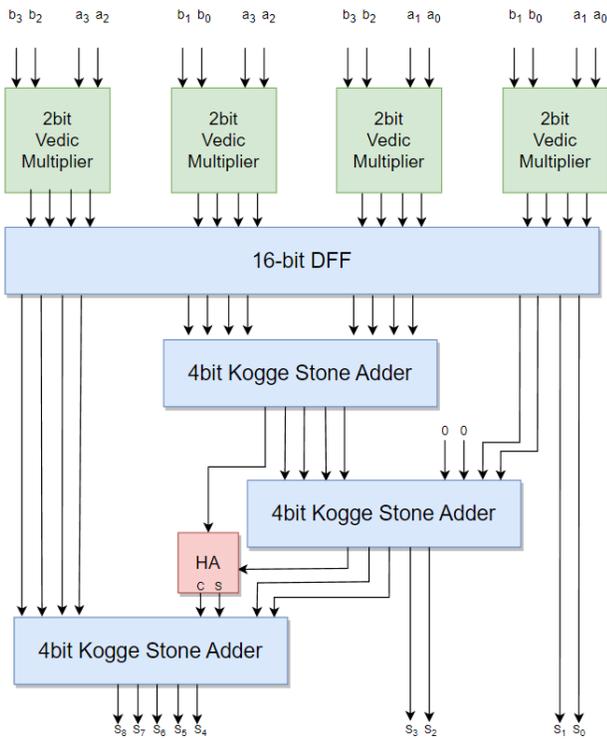


Fig. 3. Block Diagram of 4-bit Pipelined Vedic Multiplier with KSA PPA

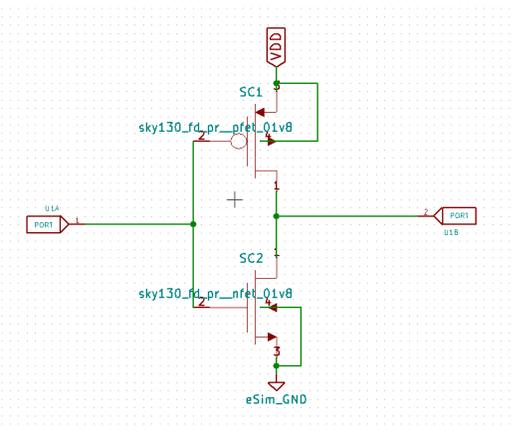


Fig. 4. Schematic of NOT gate

With the **Half Adder** and **AND** gate the 2-bit Vedic Multiplier is design and schematic for the same is shown in Fig. 8.

B. Digital Designing Part

The adder used in this is a parallel prefix version of the **Carry Look Ahead Adder (CLA)** i.e. **Kogge Stone PPA**. It is the fastest adder which focuses on design time and is said to be a good alternative for high performance applications. The speedy nature of KSA is because of minimum logic depth and restricted fan-out. In KSA, parallel advance will give scope to

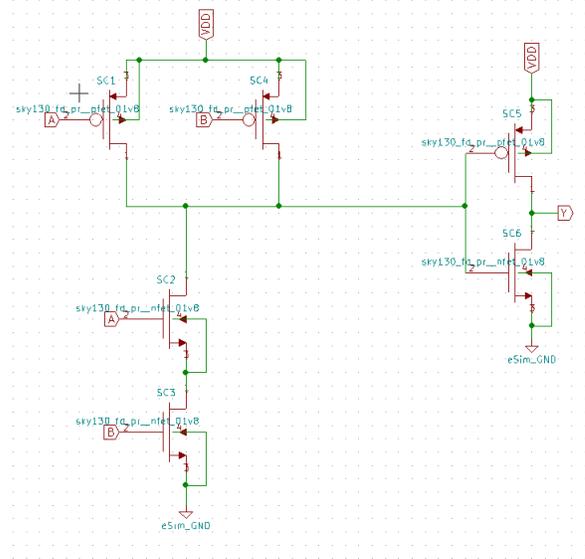


Fig. 5. Schematic of AND gate

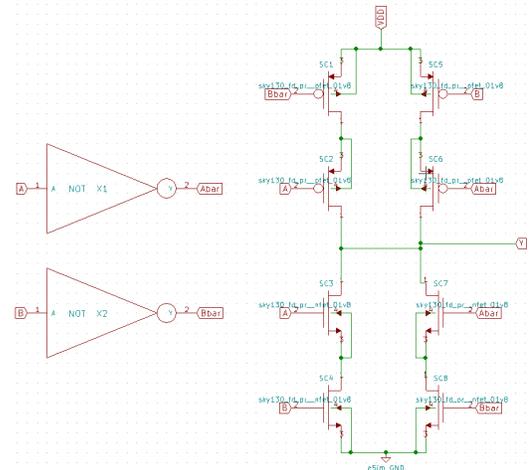


Fig. 6. Schematic of XOR gate

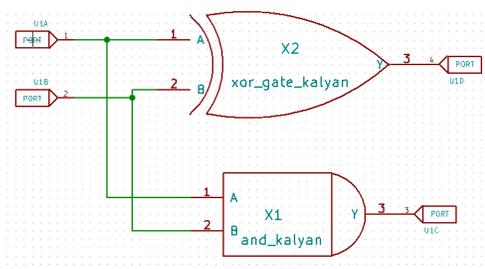


Fig. 7. Schematic of Half Adder

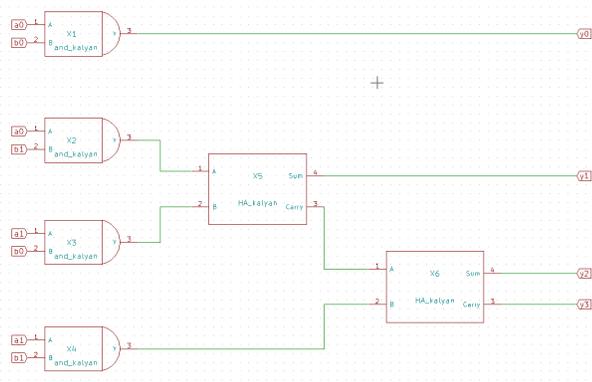


Fig. 8. Schematic of 2-bit Vedic Multiplier

generate fast carry for intermediate stages. Block diagram of KSA is shown in Fig. 9. The code for all these modules is present in the shared material.

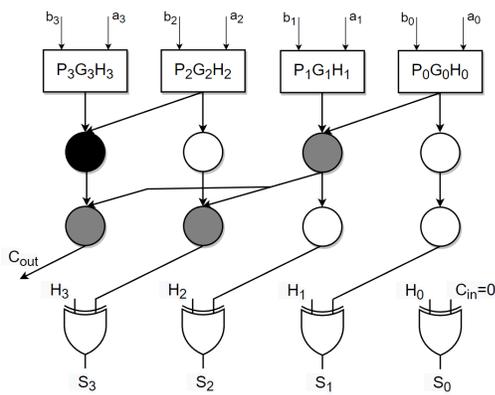


Fig. 9. Block Diagram for 4-bit Kogge Stone Adder

Black and Grey circle in Fig. 9 can be implemented as in Fig. 10. And the white circle are just simple wires shown in the figure for symmetricity.

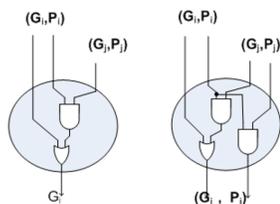


Fig. 10. Block Diagram for Black and Grey circles

This KSA is simulated in makerchip and the simulated result is shown in Fig. 11. The input a and b are asserted with random number by makerchip (in this example a = 0xF and b = 0x9) which results 0xF + 0x9 = 0x18. Hence the KSA is verified and now we can use it in eSim for our mixed signal design.

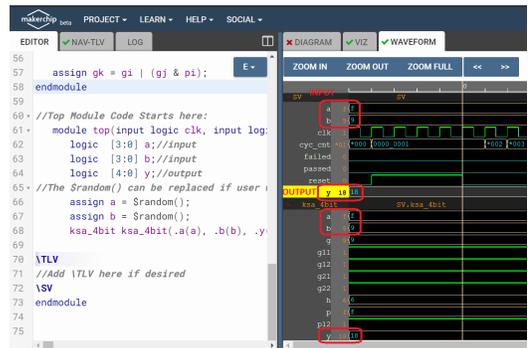


Fig. 11. Makerchip simulation for KSA

IV. OVERALL SCHEMATIC AND SIMULATION RESULTS

Overall schematic for pure combinational and pipelined design is shown in Fig. 12 Fig. 13 respectively with just a simple difference of 16-bit DFF.

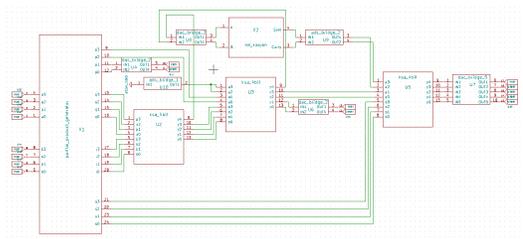


Fig. 12. Schematic of Combinational Vedic Multiplier

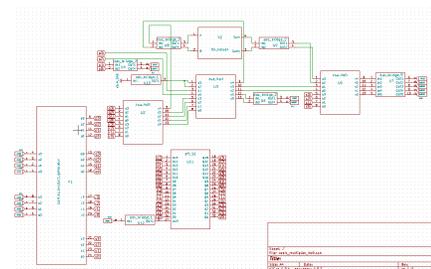


Fig. 13. Schematic of Pipelined Vedic Multiplier Subcircuit

For testing of the above sub-circuits, schematics in Fig. 14 and Fig. 15 has been made.

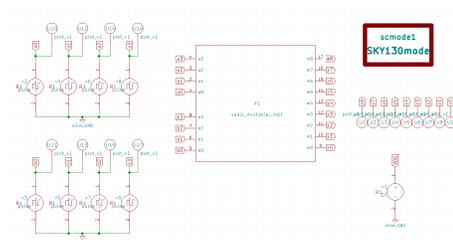


Fig. 14. Schematic for testing the combinational design

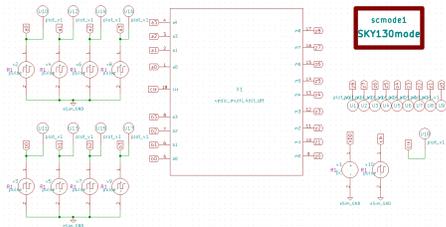


Fig. 15. Schematic for testing the pipelined design

A. Simulation Results of Combinational Design

Input for Combinational Design:

Input “a” is 10(0b1010) for t = 0 to 1 sec and then 7(0b0111) for t = 1 to 2 sec which is shown in Fig. 16.

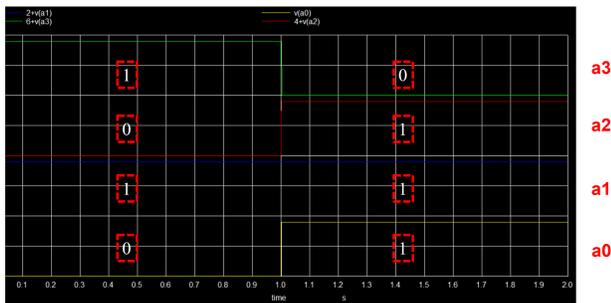


Fig. 16. Waveform of input port “a”

Input “b” is 12(0b1100) for t = 0 to 1 sec and then 7(0b0111) for t = 1 to 2 sec which is shown in Fig. 17.

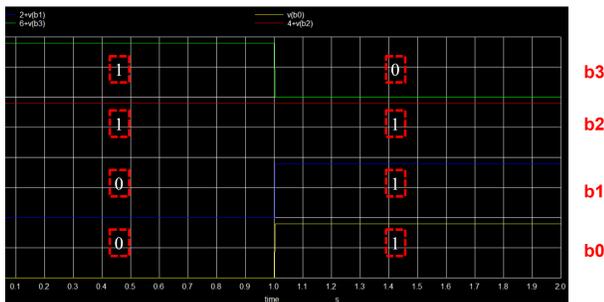


Fig. 17. Waveform of input port “b”

Output for Combinational Design:

Output “z” is 120(0b1111000) = 10 * 12 for t = 0 to 1 sec and then 49(0b110001) = 7 * 7 for t = 1 to 2 sec which is shown in Fig. 18.

B. Simulation Results of Pipelined Design

Input for Pipelined Design:

Input “a” is 10(0b1010) for t = 0 to 1 sec, 7(0b0111) for t = 1 to 2 sec and then 11(0b1011) for the rest which is shown in Fig. 19.

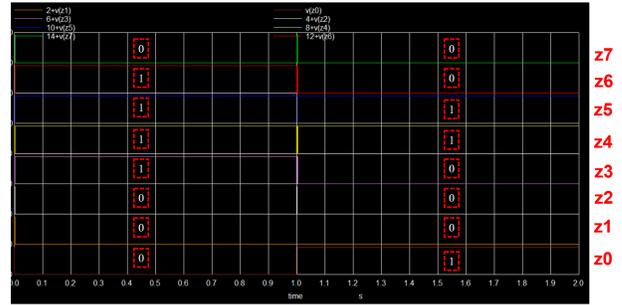


Fig. 18. Waveform of output port “z”

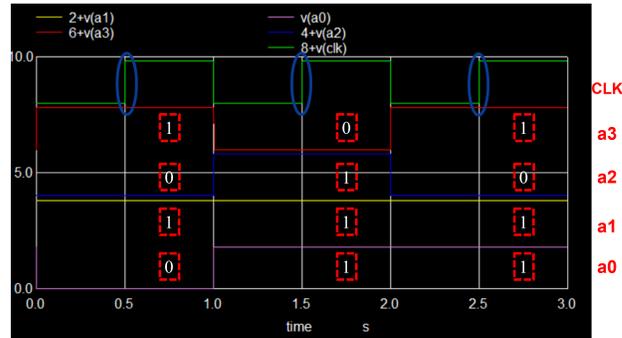


Fig. 19. Waveform of input port “a”

Input “b” is 12(0b1100) for t = 0 to 1 sec and then 7(0b0111) for t = 1 to 2 sec which is shown in Fig. 20.



Fig. 20. Waveform of input port “b”

Output for Pipelined Design:

Output “z” is 120(0b1111000) = 10 * 12 for t = 0 to 1 sec and then 49(0b110001) = 7 * 7 for t = 1 to 2 sec which is shown in Fig. 21.

REFERENCES

- [1] “Kogge Stone Adder” https://en.wikipedia.org/wiki/Kogge-Stone_adder
- [2] T. Sutra, “Design of Vedic multiplier using Urdhva Tiryagbhyam Sutra” <https://www.semanticscholar.org/paper/Design-of-Vedic-multiplier-using-Urdhva-Tiryagbhyam-Sutra/29e50274fddab42ec935af7a39aac92080c9e6c>

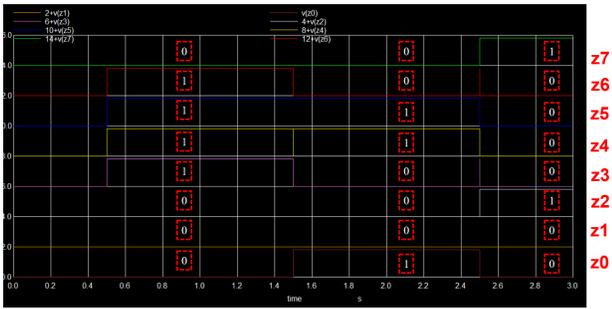


Fig. 21. Waveform of output port "z"