

RONOUS DOWN COUNTER WITH RING OSCILLATOR AS CLOCK

Soham Sen

National Institute of Technology Silchar

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Abstract

The paper constitutes the design and analysis of a 3 bit Down Counter. This circuit uses Ring Oscillator as clock. It mainly focuses on the mixed signal circuit design. In this design, a 3 bit down counter is implemented using Verilog code and ring oscillator is implemented using CMOS logic. As computer system consists of sequential circuits mostly, it is very important to design sequential circuits effectively and flawlessly for ensuring least power dissipation and architectural simplicity. Counters are very important segments of sequential circuit system. In this paper we have proposed a design scheme to develop a down counter with ring oscillator as clock input.

1 Circuit Details

A Down Counter is an application of shift registers. N number of flipflops are required for N bit counter. For a 3 bit counter, 3 Flipflops are required. It counts from 7 down to 0. Here T flipflop is used. Synchronous counter has one global clock which drives each flipflop so output changes in parallel. CMOS Ring oscillator is the most popular oscillator topology in recent days due to its CMOS technology advantages. In this architecture the last inverter's output is connected to the first inverter's input through a feedback path. It is known as the ring oscillator because of inverters are connected in ring fashion. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator.

$$\text{Time period of ring oscillator}(T)=2*n*T_d$$

$T_d = \text{Propagation delay of each inverter}$

Frequency of ring oscillator(f)= $1/T$

n=Number of inverters

The frequency of oscillation is dependent on the number of stages and delay time of each inverter stage.

2 Circuit Design

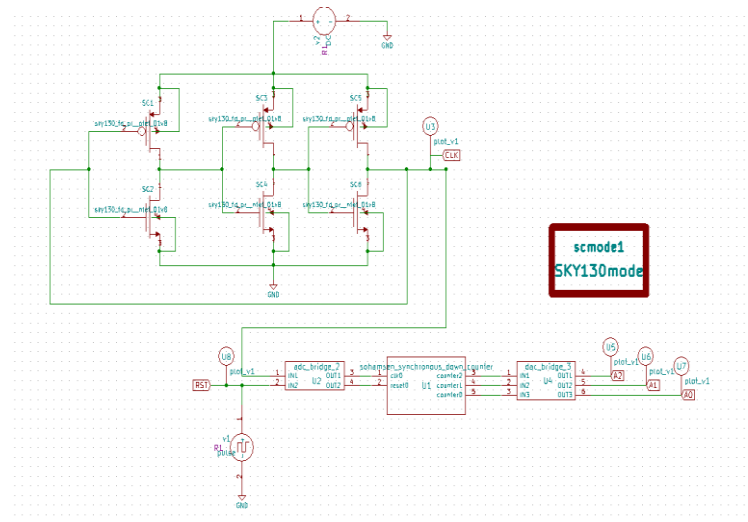


Figure 1

3 Output Waveforms

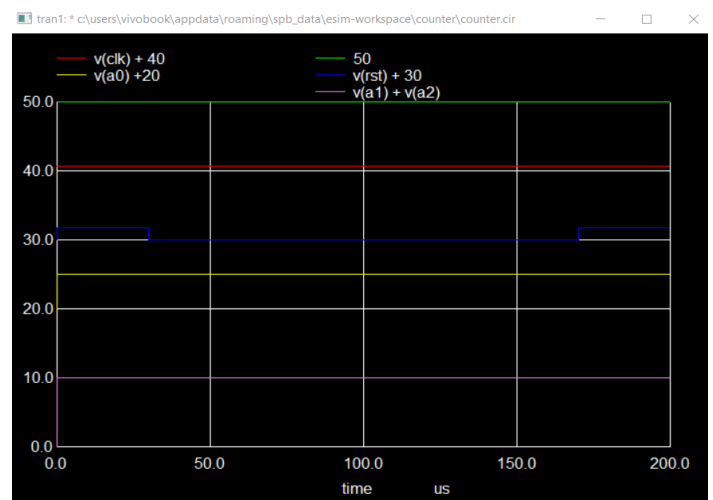


Figure 2

Reference Paper/Journals

- [1] CMOS Inverter Ring Oscillator. shorturl.at/flMW7
[2] Digital Circuits - Counters. shorturl.at/HKV23