

3-bit Synchronous up counter with buffered reset

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Abstract— Counters are digital circuits widely used in various applications like counting, frequency divisions, memory increment in the registers, etc. This abstract describes the implemented design of a 3-bit up counter where the reset is buffered using a CMOS inverter buffer for better performance.

I. REFERENCE CIRCUIT DETAILS

The circuit is designed on SkyWater 130 pdk on esim software. The asynchronous reset for the counter is specially buffered to avoid the issue of weak reset which could lead to the counter not getting reset when required by the user. The buffer circuit is designed using connecting back-to-back 2 CMOS digital inverters [1][2][3] to keep the buffer area efficient yet good in performance.

II. REFERENCE CIRCUIT DESIGN

The designed schematic is shown in Fig 1.

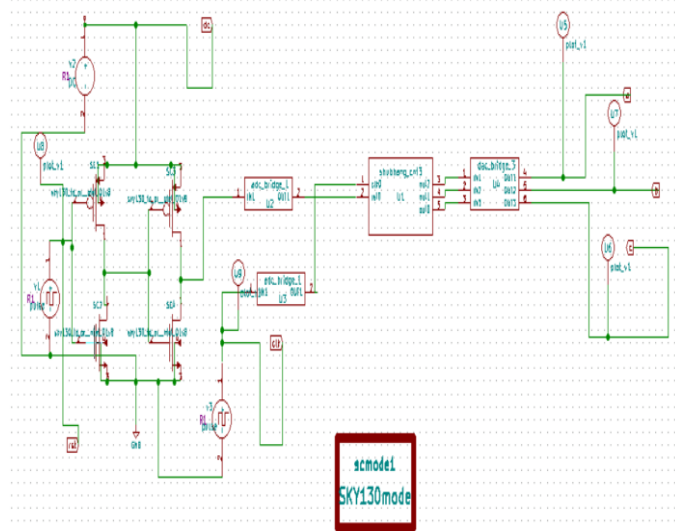


Fig 1: Circuit Schematic

III. REFERENCE WAVEFORM

The operation of the counter along with the enabling of synchronous reset is shown in Fig 2.

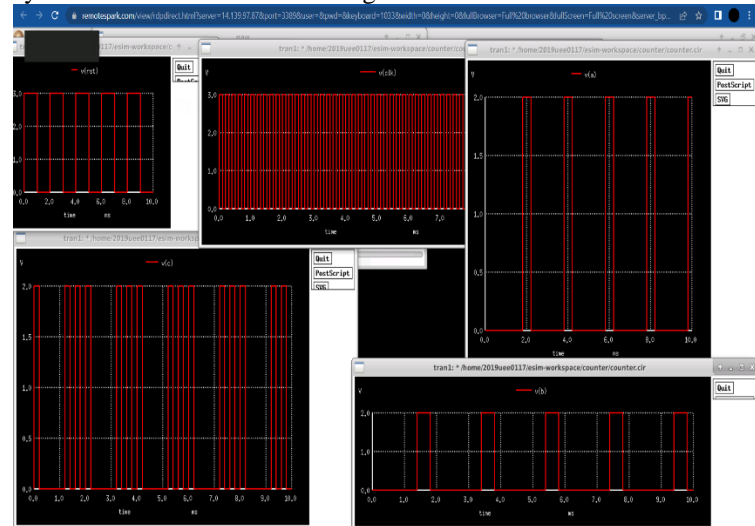


Fig 2: Obtained Circuit Waveforms

REFERENCES

- [1] Maekawa, Tomoaki & Amakawa, Shuhei & Ishihara, Noboru & Masu, Kazuya. (2009). Design of CMOS inverter-based output buffers adapting the Cherry-Hooper broadbanding technique. 511 - 514. 10.1109/ECCTD.2009.5275025.
- [2] Mariyamol, p.p & Aswathy, N.. (2016). CMOS Buffer Design Approach for Low Power and Lower Delay SRAM Design. Procedia Technology. 25. 481-488. 10.1016/j.protcy.2016.08.135.
- [3] Thomas L. Floyd “Digital Fundamentals”, 11th ed global edition, pp. 507-527