SR Flip Flop to JK Flip Flop

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***Abstract* – In this paper we are presenting the conversion of SR Flip Flop to JK Flip Flop using 45 nm technology. Flip Flops are widely used in electronic circuit as they have frequency division property. Flip Flops are widely used in counters, registers and in any data transfer block. The design we are going to use for this conversion is the SR Flip Flop will be made of analog block and the gates which provide input to the SR Flip Flop will be made of digital block.**

***Keywords* – SR Flip Flop, JK Flip Flop, Verilog, CMOS**

I. REFERENCE CIRCUIT INTRODUCTION

In Fig.1 we can see that the the actual input of the SR Flip Flop are S and R, the external inputs of the SR Flip Flops are J and K. We will see a total of 8 combinations as input out of which some values are don't care in S and R. We are able to draw this circuit by simplifying the K-Map as shown in Fig.2. The K-Map is derived from the the truth table of JK Flip Flop and excitation table of SR Flip Flop.

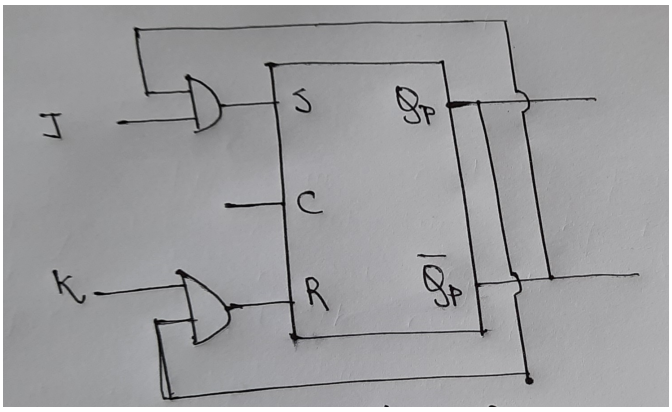

Fig. 1. Block Diagram of JK Flip Flop to SR Flip Flop [1]

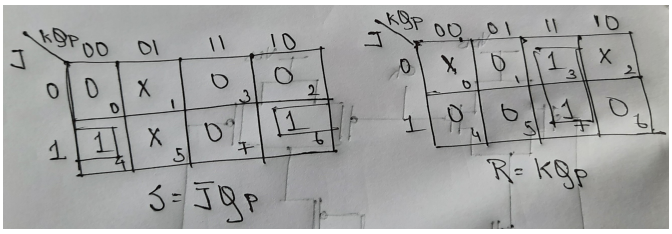

Fig. 2. K-Map Simplification for the block diagram

II. REFERENCE CIRCUIT DESIGN

In Fig.3 we see the implementation of the SR Flip Flop using CMOS.This part of our circuit will be the analog circuitry block. The circuit designed is a 45 nm circuit as shown in [2].

The digital block implementation using Verilog Hardware Description Language will be the used to design the AND gate which feeds input to the the S and R input of the CMOS based SR Flip Flop.

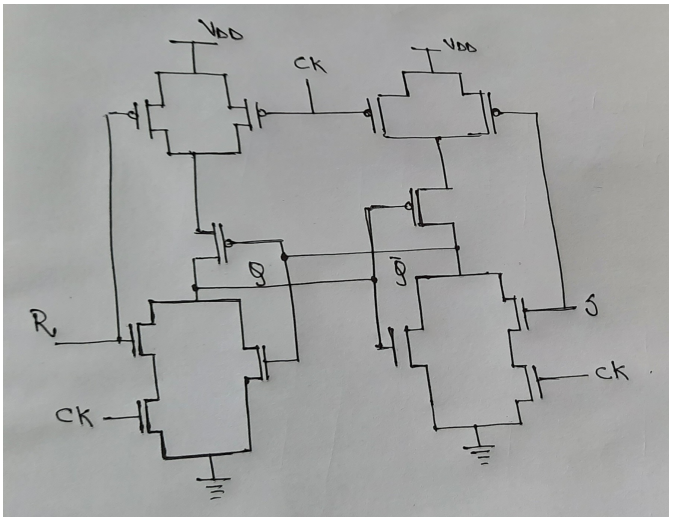

Fig. 3. CMOS Implementation of SR Flip Flop

III. REFERENCE CIRCUIT WAVEFORM

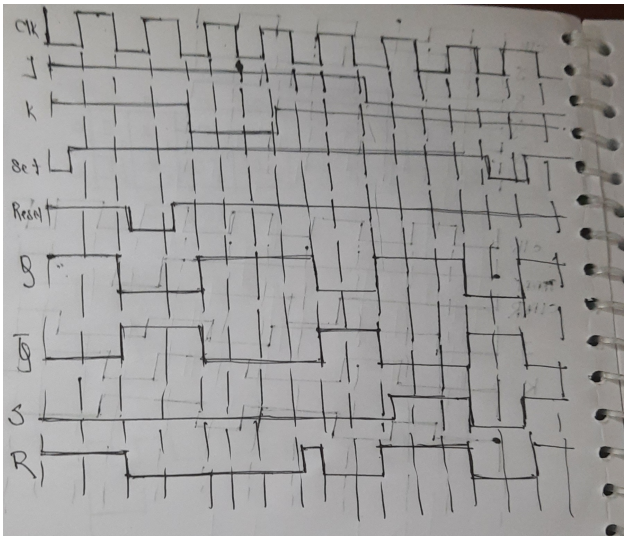

Fig. 4. Waveform of conversion of JK Flip Flop to SR Flip Flop

IV. REFERENCES

[1] Website: https://www.circuitstoday.com/flip-flop-conversionSRtoJK

[2] Prabhu Deva Kumar, Seelam Vasavi Sai and Venkat, Pagadala and Nayini, Lokesh, Implementation and Designing of Low Power SR Flip-Flop Using 45NM CMOS Technology (August 30, 2017). http://dx.doi.org/10.2139/ssrn.3029181