

# FREQUENCY DIVIDER USING ASTABLE MULTIVIBRATOR AND COUNTER

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## Abstract:

I am going to introduce a design of frequency divider using astable multivibrator and counter. For frequency dividing we can use both synchronous or asynchronous and upcounter or downcounter. In this I choose asynchronous MOD-10 upcounter. Components used in this design are IC741 (opamp), Resistors, Capacitor, NAND gate, JK-flipflops.

## Reference Circuit Details:

In astable multivibrator, initially capacitor voltage is 0V. the capacitor charges and discharges via 'R' with a time constant  $\tau = RC$ . Astable multivibrator generates a clock pulse with a time period

$$T = 2RC \ln \left( \frac{1+\beta}{1-\beta} \right) \quad \text{where } \beta = \left( \frac{R_1}{R_1+R_2} \right).$$

In MOD10 upcounter, all the JK-flipflops are connected to logic high (1) to toggle. MOD10 upcounter counts from 0 to 9. Usually 4-bit counter counts from 0 to 15, but we need to count upto 9 only. so, in the Counter circuit Q3 and Q1 are connected to NAND gate and output of it is connected to asynchronous clear input for four JK-flipflops.

Let us assume that the clock pulse generated by the astable multivibrator having the time period T as shown in the fig-2. The output of the astable multivibrator is given to the MOD10 upcounter as clock. The clock pulse at the output of first JK-flipflop's (Q<sub>0</sub>) time period increased by twice and the clock pulse at the output of the second JK-flipflop's (Q<sub>1</sub>) time period increased by 4 times. The clock pulse at the output of the third JK-flipflop's (Q<sub>2</sub>) time period increased by 8 times. The clock pulse at the output of the fourth JK-flipflop's (Q<sub>3</sub>) time period increased by 10 times.

$$\text{Frequency (F)} = \frac{1}{\text{Time period}(T)}$$

Therefore, we attain the frequency at the output of the design is equal to  $\frac{1}{10T}$ .

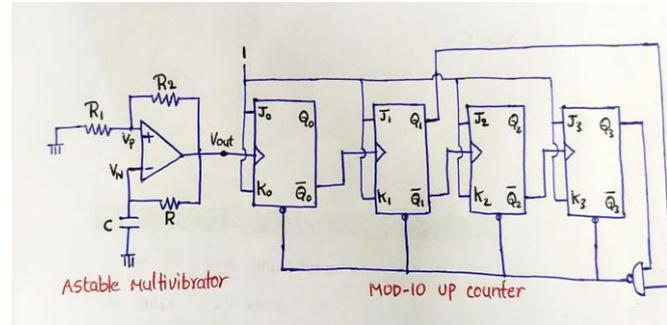


Figure 1

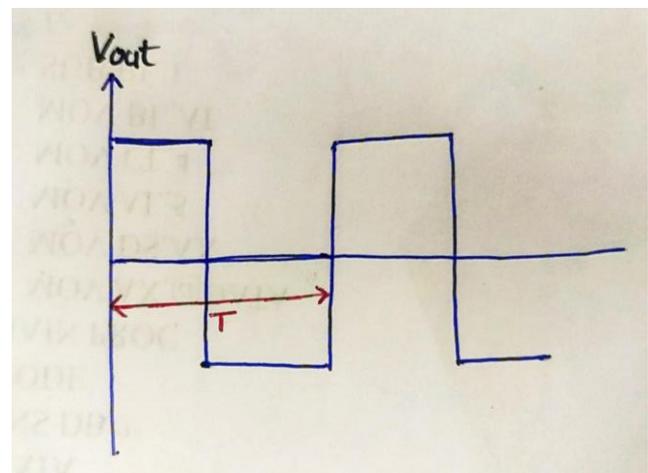


Figure 2

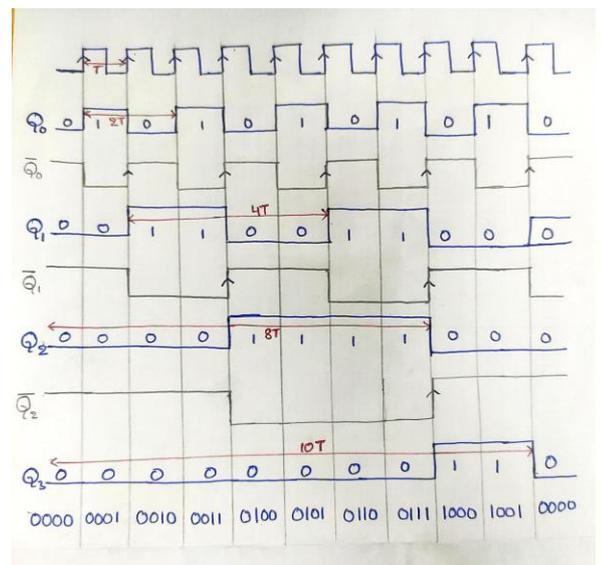


Figure 3