Half adder using Mixed signals

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***Abstract*—In this project, half adder is designed by mixed signals using SKY130mode. The design includes both analog and digital circuits. Digital block i.e. 2-bit counter, NOT, BUFFER, EX-NOR gates is designed using Makerchip-NgVeri and analog block i.e. NAND gate is designed using Ngspice. The pulses are given to a 2-bit counter as an analog signal. This counter generates specific sequences which get added with the adder circuit. Adder circuit again consists of mixed signal i.e. EX-OR gate for SUM and Complementary metal oxide semiconductor (CMOS) NAND gate with NOT gate for CARRY.**

Keywords—mixed, SKY130mode, half adder, Makerchip-NgVeri, Ngspice, CMOS

I. Reference Circuit Details

Fig.1 shows the schematic of half adder in which both analog and digital circuits are used. The 2-bit counter is designed using Makerchip-NgVeri by writing the Verilog code for it [1]. The analog signal such as *clock* and *reset* pulse are given to a 2-bit counter via ADC bridge. As name suggests, it counts the number of clock pulses. This counting can be done in a sequential manner to count the number of clock pulses or in a random manner to generate a specific sequence. As shown in Fig.2 the output of counter *A* and *B* generates the specific sequence like 00, 10, 01, 11, 00… and so on [1].

A logic circuit for the addition of two 1-bit numbers is referred to as a half adder [2]. Table.1 shows the truth table for the same.

A	B	SUM	CARRY
0	0	*0*	*0*
0	1	*1*	*0*
1	0	*1*	*0*
1	1	*0*	*1*

Table.1 Truth table of half adder

Sum = A **EX-OR** B, Carry = A **AND** B

As shown in Fig.1, the circuit is designed using mixed signals. *CARRY* is designed with CMOS NAND gate, NOT gate & *SUM* is designed using only EX-OR gate. The generated sequence from 2-bit counter will be used as inputs to adder circuit as *A* and *B*. Fig.2 shows the output waveforms for *SUM* and *CARRY*.

The EX-OR gate is designed using Makerchip-NgVeri by writing the Verilog code for it. The signals *A* and *B* from the counter are cascaded with EX-OR gate to get *SUM*. The buffers are used in this design for proper alignment in the output. It helped in removing the unwanted spikes in output waveform.

Two inputs CMOS NAND gate requires two PMOS and two NMOS. So CMOS NAND gate is designed by using sky130 pfet_01v8 and sky130 nfet_01v8. The output of NAND gate is given to NOT gate via DAC bridge to get *CARRY*. As said NOT gate is designed using Makerchip-NgVeri by writing the Verilog code for it. Here also buffers are used for same purpose.

II. Reference Circuit

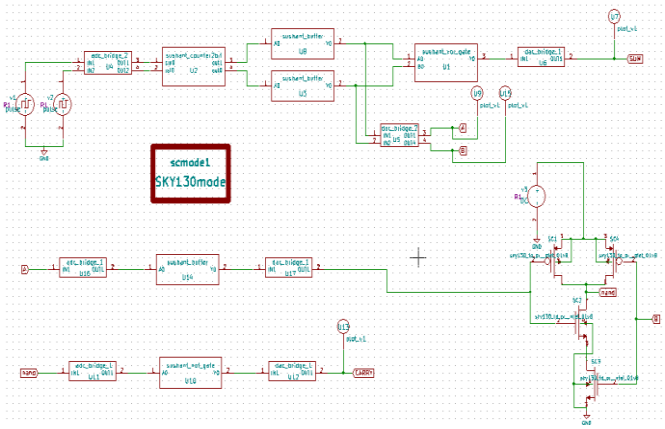

Fig.1 Schematic of half adder using mixed signals.

III. Reference Waveforms

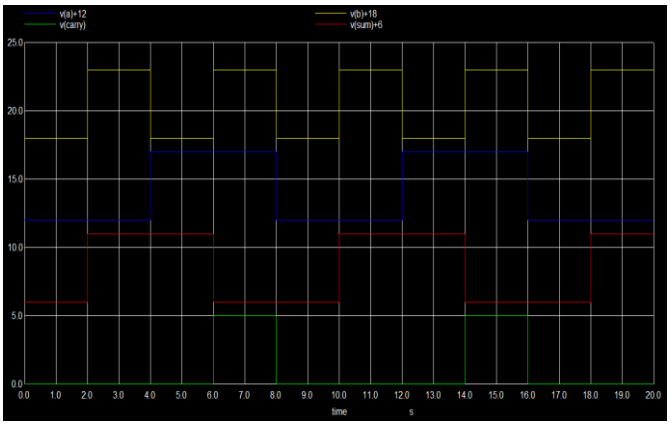

Fig.2 Waveforms of half adder using mixed signals.

IV. References

[1] https://www.vsdiat.com.

[2] Book by R P Jain, Modern Digital Electronics.