Half adder using Mixed signals

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***Abstract*—The literature survey is on half adder using mixed signals. The proposed circuit design includes both analog and digital circuits. Zero crossing detector (ZCD) is used to generate the square waves, which is fetched to 2-bit counter. These 2-bit numbers get added with the adder circuit. Adder circuit again consist of mixed signal i.e. Complementary metal oxide semiconductor CMOS NAND gate (analog) with NOT gate (digital) for CARRY and EX-OR gate (digital) for SUM.**

Keywords—mixed, half adder, ZCD, 2-bit counter, CMOS

I. Reference Circuit Details

Fig.1 shows the block diagram for half adder. It consists of Zero crossing detector (ZCD), 2-bit counter, Complementary metal oxide semiconductor (CMOS) NAND gate with digital NOT and EX-OR gate. ZCD works on the principle of comparator using OPAMP and gives square wave as output. ZCD has the ability to detect the change in sinusoidal waveform [1].

Whenever input to inverting terminal is greater than non inverting terminal, ZCD will give LOW output and when input to inverting terminal is less than non inverting terminal ZCD will get HIGH output, in this manner will get the output in the form of square.

Here, input V_{in} (sine wave) is applied on inverting terminal and $V_{ref} = 0$ is applied on non-inverting terminal as shown in Fig.1. In this case, for first half of sine wave output goes LOW and for second half output goes HIGH as shown in Fig.2.

The ZCD is cascaded with 2-bit counter wherein output of ZCD is fetched to counter as clock with an external reset pulse as shown in Fig.1. As name suggests, it counts the number of clock pulses. This counting can be done in a sequential manner to count the number of clock pulses or in a random manner to generate a specific sequence. As shown in Fig.2 the output of Y_1 and Y_2 generates the specific sequence like 00, 10, 01, 11, 00… and so on [2].

A logic circuit for the addition of two 1-bit numbers is referred to as a half adder [3]. Table.1 shows the truth table for the same.

A	B	SUM	CARRY
0	0	*0*	*0*
0	1	*1*	*0*
1	0	*1*	*0*
1	1	*0*	*1*

Table.1 Truth table of half adder

Sum = A **Ex-OR** B, Carry = A **AND** B

As shown in Fig.1, the proposed circuit is designed using mixed signals. CARRY is designed with CMOS NAND gate, NOT gate & SUM is designed using only EX-OR gate. The generated sequence from 2-bit counter will be used as inputs to adder circuit as A and B. Fig.2 shows the output waveforms for SUM and CARRY.

II. Reference Circuit

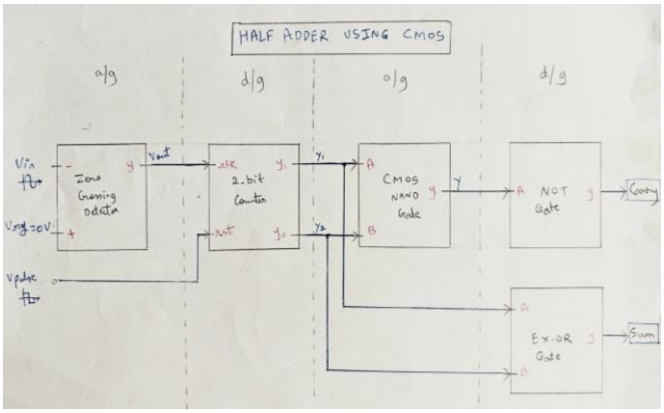

Fig.1 Block diagram of half adder using mixed signals.

III. Reference Waveforms

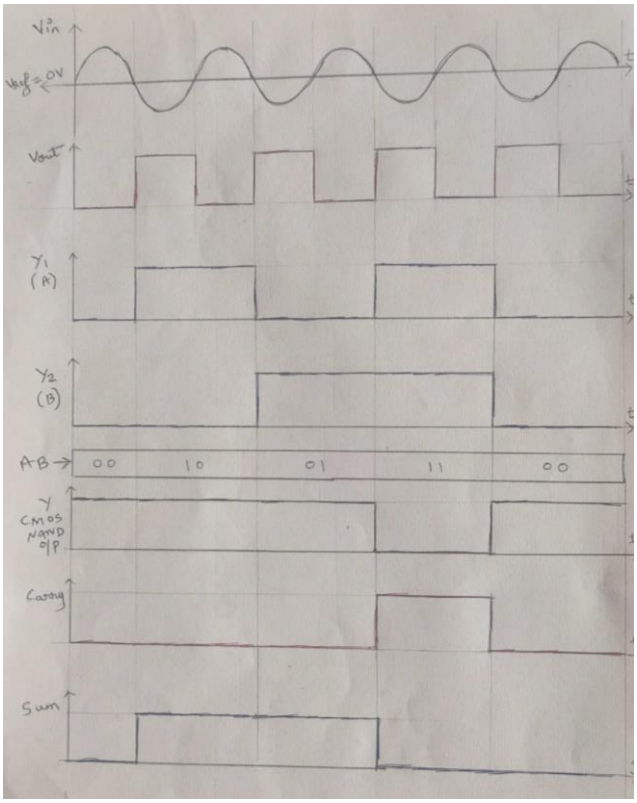

Fig.2 Proposed Waveforms.

IV. References

[1] Book by Ramakant A. Gayakwad, Op-amps and linear integrated circuit technology.

[2] https://www.vsdiat.com.

[3] Book by R P Jain, Modern Digital Electronics.