Frequency Doubler using Mixed Signal Circuit

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Abstract- Frequency doubler circuits are extensively used in high frequency and low power consumption applications where the input signal frequency is relatively low such as a low clock frequency. While there are several methods implemented to generate a frequency doubler like PLL, I have developed a mixed signal circuit with considerably low hardware overhead, composing of an astable multivibrator to generate a Pulse Width Modulating signal, a 90 degrees phase shift circuit for the PWM signal and an XOR gate written in Verilog code to obtain the final frequency doubled output signal.

Keywords—frequency doubler, phase shift

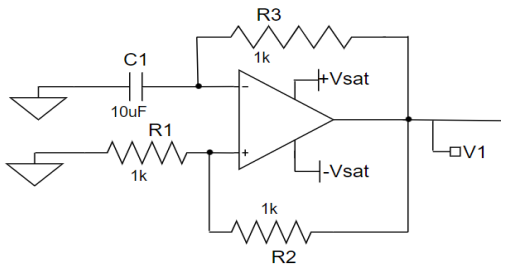
I. CIRCUIT DETAILS

The overall design will include a PWM signal V1 generated by an astable multivibrator circuit, which will be followed by a phase shift stage that produces an output V2 equal to V1 phase shifted by 90 degrees. Both these stages are developed using e-Sim and Sky130 PDK as analog part of the mixed signal circuit. Then, V1 and V2 are fed as inputs to an XOR logic gate written in Verilog code. The final output V3 out of the XOR gate will be a PWM signal with frequency equal to double the frequency of V1. This will correspond to the digital part of the project. This is how I have implemented a frequency doubler circuit using a mixed signal model. The block wise descriptions are briefly shown below for reference.

II. REFERENCE CIRCUITS

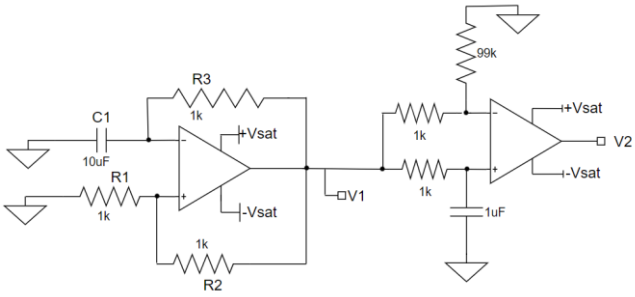
A. *PWM Signal using Astable Multivibrator*

The circuit produces output V1 equal to +-Vsat of the op-amp. The high and low time periods of the PWM signal is equal to the charging and discharging times of the capacitor respectively as shown in Fig 1. As the charging and discharging path for the capacitor is the same, the duty cycle of the output PWM signal will be 50%.



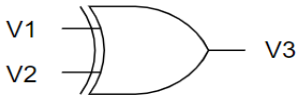
B. *Phase Shifting Circuit*

The following circuit is essentially a comparator that adds a delay equal to half the high time period of V1. This actually introduces a phase shift of 90 degrees to the PWM signal V1.



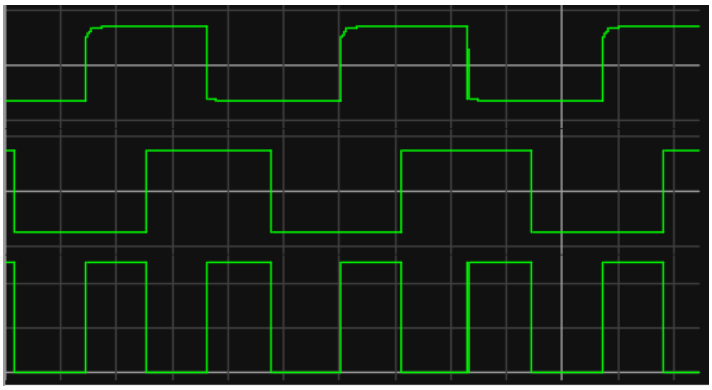
C. *XOR-ed Output with double frequency*

The final output V3 is obtained by XOR-ing the two signals V1 and V2. This part of the model is simulated in Verilog and used as a NgVeri block in eSim. If the frequency of V1 (and V2) is f, the frequency of V3 is observed to be 2f.



III. REFERENCE WAVEFORM

A. he below plots represent V1, V2 and V3 stacked from top to bottom. V1 corresponds to the actual PWM signal, V2 corresponds to the 90 degrees phase shifted version of V1 and V3 is the XOR-ed output of V1 and V2. We can observe that the frequency of V3 is clearly double that of V1 and V2.



IV. REFERENCES

A. https://www.maximintegrated.com/en/design/technical-documents/app-notes/3/3327.html