# Frequency Doubler using Mixed Signal Circuit

Hrittika Ghosh, Jadavpur University

***Abstract- Frequency doubler circuits are extensively used in high frequency and low power consumption applications where the input signal frequency is relatively low such as a low clock frequency. While there are several methods implemented to generate a frequency doubler like PLL, I have developed a mixed signal circuit with considerably low hardware overhead, composing of an astable multivibrator to generate a Pulse Width Modulating signal, a 90 degrees phase shift circuit for the PWM signal and an XOR gate written in Verilog code to obtain the final frequency doubled output signal.***

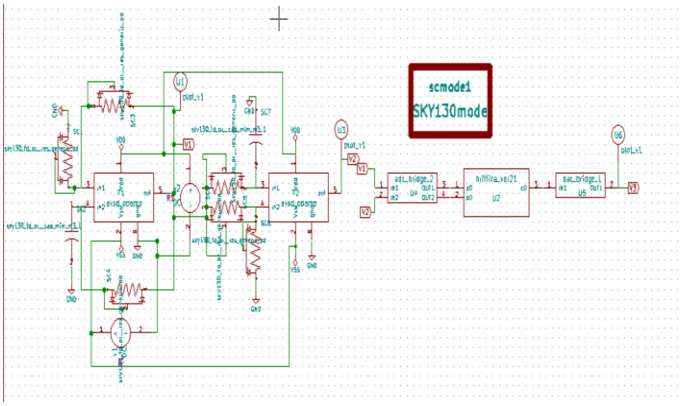
***Keywords—frequency doubler, phase shift***

## I. CIRCUIT DETAILS

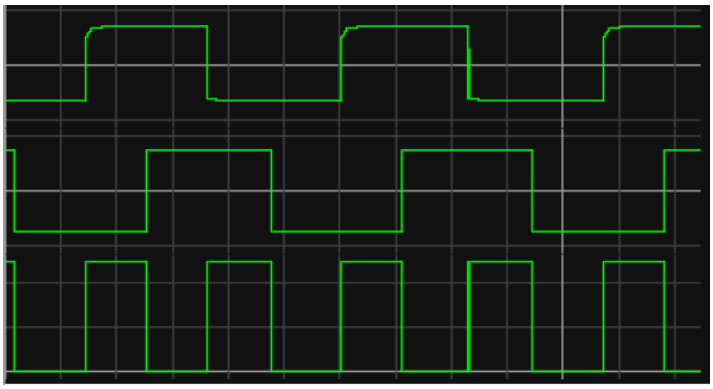
The overall design will include a PWM signal V1 generated by an astable multivibrator circuit, which will be followed by a phase shift stage that produces an output V2 equal to V1 phase shifted by 90 degrees. Both these stages are developed using e-Sim and Sky130 PDK as analog part of the mixed signal circuit. Then, V1 and V2 are fed as inputs to an XOR logic gate written in Verilog code. The final output V3 out of the XOR gate will be a PWM signal with frequency equal to double the frequency of V1. This will correspond to the digital part of the project. This is how I have implemented a frequency doubler circuit using a mixed signal model. The block wise descriptions are briefly shown below for reference.

## II. REFERENCE CIRCUIT

The reference circuit consists of three main stages: an astable multivibrator to generate a PWM signal, a phase shift circuit and a 2 input XOR block implemented using Verilog.




## III. REFERENCE WAVEFORMS.



## IV. REFERENCES

*A.* [https://www.maximintegrated.com/en/design/technical-documents/app-notes/3/3327.html](https://www.maximintegrated.com/en/design/technical-documents/app-notes/3/3327.html)