

# Design of a Mix-signal Frequency Divider

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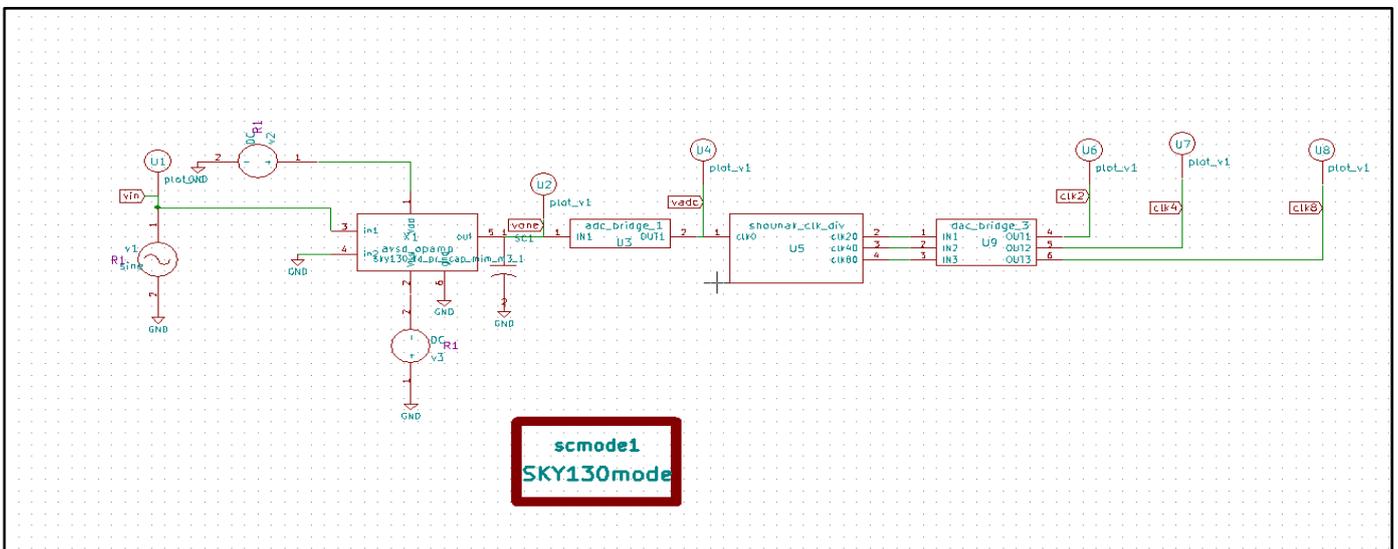
**Abstract** --- A frequency divider circuit using Op-amp and 3-bit asynchronous up counter is proposed in this paper for getting different frequency waveform at different stage of this circuit. The purpose of the circuit is to get divided frequency signal for a given frequency. We can generate desired frequency square wave from Opamp that signal can be fed to counter circuit as a clock input and later at each stage of counter circuit output, we can get desired divided frequency. This way of designing satisfies the criterion of a mix signal design where astable multivibrator act as an analog circuit and counter act as a digital circuit.

**Keywords** --- Mix signal frequency divider, 3 stage frequency divider.

## 1. Reference Circuit Details

The circuit shows the proposed design of the circuit. It consists of astable multivibrator made of Op-Amp circuit with a load capacitance 'C'. Here all component and subcircuit use with Skywater open Pdk 130nm. Here avsd\_opam is used to generate the square wave at the U2 node then it is converted to digital wave by an ADC bridge – 1 and fed into a clock divider module which is designed using Verilog, Makerchip and Ngveri tools the input square wave used as a clock to this module and the three-output channel the input frequency divided by two, four and eight in U6, U7 and U8 node respectively. Mix-signal approach is used here to generate the frequency division.

## 2. Implemented Circuit



## 3. Verilog Codes:

```
module shounak_clk_div(input clk, output clk2,clk4,clk8);
reg [2:0]b=3'b000;

always @ (posedge clk)
begin
    b=b+1'b1;
end
assign clk2=b[0];
assign clk4=b[1];
```

```
assign clk8=b[2];
```

```
endmodule
```

#### 4. Implemented Waveforms:

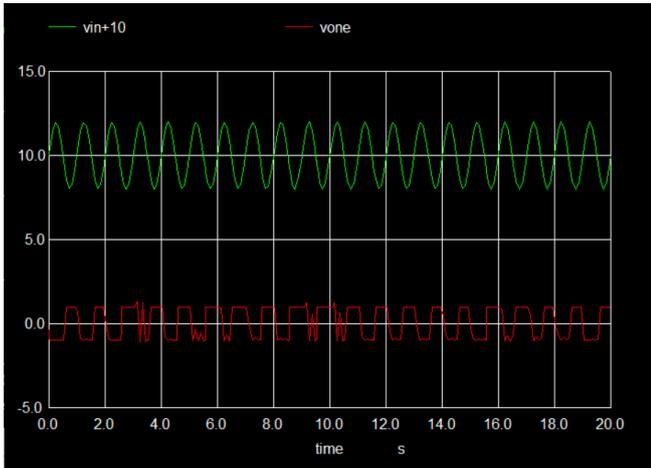


Fig 1: Sine wave to square wave

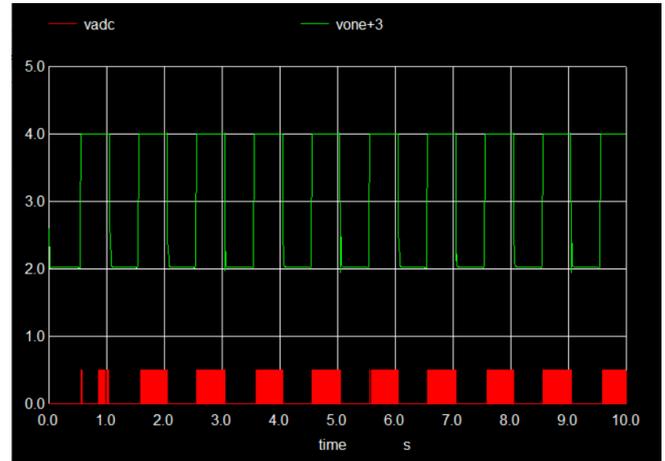


Fig 2: square wave to clock input

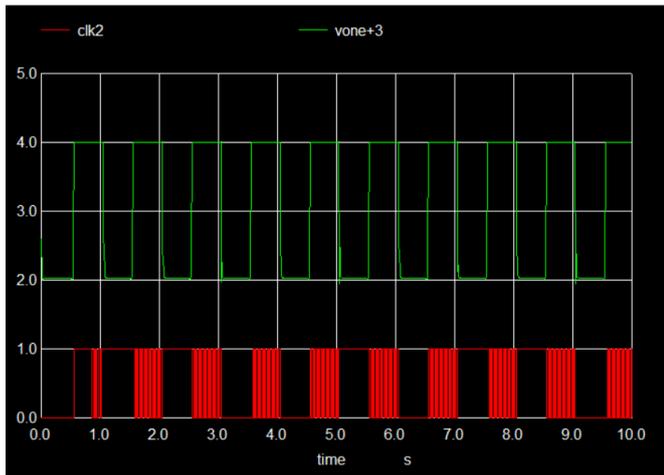


Fig 3: clock input divided by 2

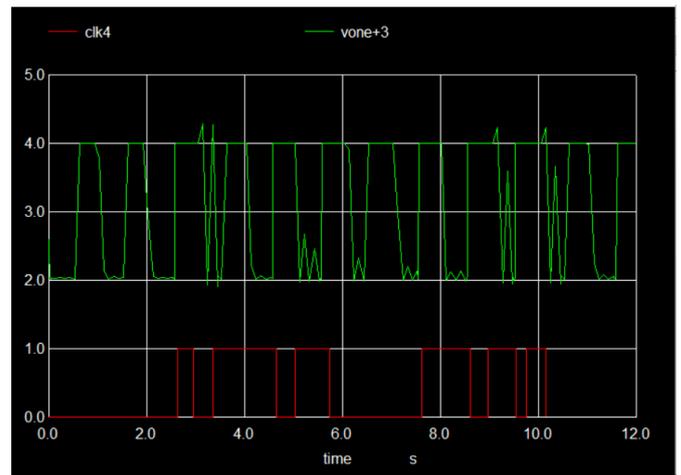


Fig 4: clock input divided by 4

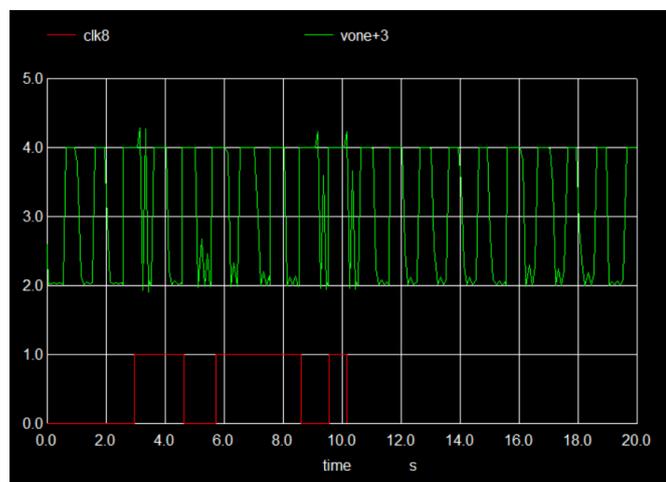


Fig 5: clock input divided by 8

## 5. References:

Digital Design by M. morris mano

VSD-IAT tutorial: <https://www.vlsisystemdesign.com/>

Fosse\_IITB: <https://esim.fossee.in/home>

Skywater Open PDK: <https://skywater-pdk.readthedocs.io/en/main/>