Design of Mixed Signal FSM Sequence Detector with CMOS Inverter

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Abstract—**An FSM is an abstract machine that can exist in only one of a finite number of states at a time. A Moore FSM is one which depends only on the value of present state and not the value of input. A sequence detector is a circuit that takes an input string of bits and generates an output 'HIGH' if the target sequence has been detected. Analog input from a CMOS inverter is fed into this digital block and output is observed.**

Keywords—*CMOS Inverter, Finite State Machine, Mixed Signals, Moore FSM, Sequence Detector*
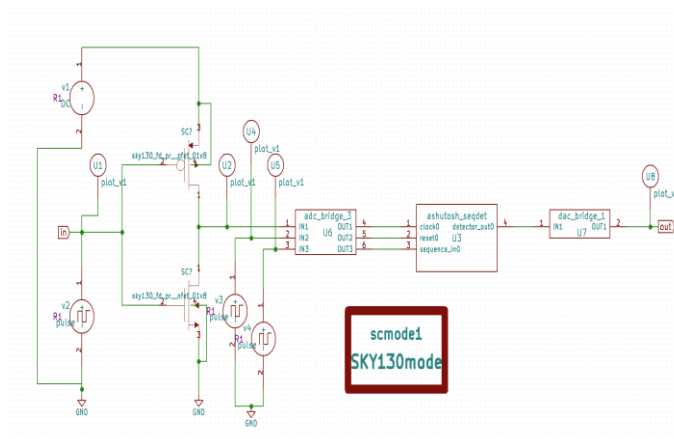
CIRCUIT DETAILS

In this paper, a Finite State Machine based sequence detector is implemented. This is a Moore based FSM, where the output is only dependent on the present state. This FSM block is a digital block consisting of three inputs, which are clock, sequence_in and reset. It has one output, the detector_out. This is coded in Verilog.

For the analog part, a CMOS inverter is implemented using MOS transistors. The voltage is supplied to the CMOS inverter. The output of the inverter is fed into an ADC block (Analog-to-Digital). The output from this block is passed as input to the FSM digital block along with additional voltage supplies for the clock and reset. The output of the FSM block will be a single output which goes high iff the required sequence is detected i.e 1011 in this case.
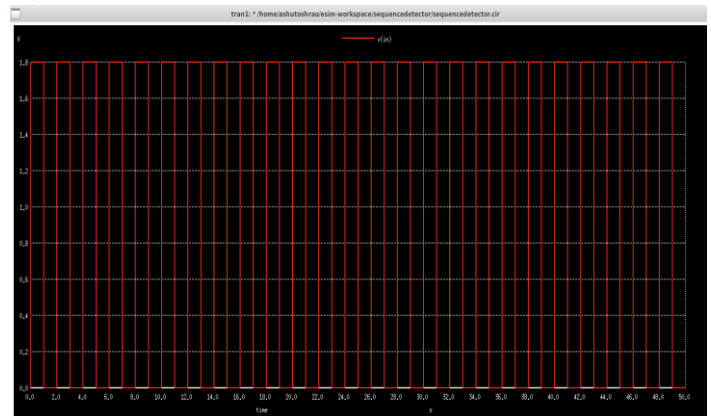
As the sequence_in is giving a stream of 010101…, the output sequence is not detected and thus the Vout is 0 as expected. As this is a 1011 sequence detector, the output will not change for any other sequence as 1011 is not included in 010101… **However, when tested with the testbench code which can be found on this project's GitHub repository, the code shows a high output when 1011 is detected.**
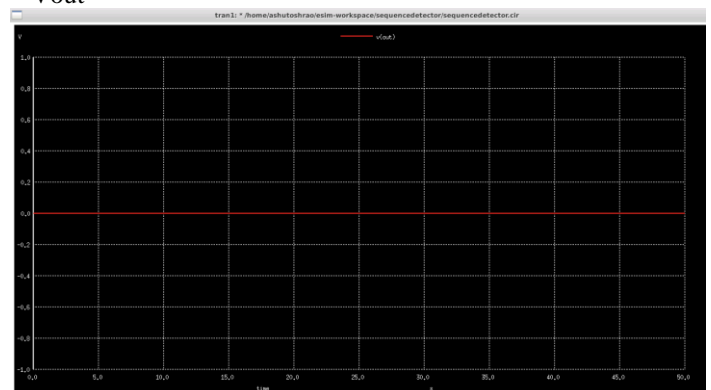
IMPLEMENTED WAVEFORMS

Vin

Vout

IMPLEMENTED DESIGN

REFERENCES

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