

DESIGN OF 4 BIT COUNTER WITH CLOCK AS INVERTER CHAIN AND LOW POWER CVSL (Cascode Voltage Switch Logic)

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Abstract- a 4 Bit up Counter is proposed with clock being generated from Inverter Chain circuit followed by Low Power Cascode Voltage Switch Logic AND Gate.

Circuit Details-

Block 1 comprises of Inverter Chain Circuits comprising of n Inverters, which act as Ring Oscillators with Frequency given by $f = 1/2nT_d$ where n is no of Inverters (is Odd) and T_d is delay of each inverter circuit.

Another Output (B) is taken from across one more terminal from the chain to get delayed waveform.

Both the output A,B are 'anded' to get a wave with lesser duty cycle, which can work as Edge Trigg Clock, the duty cycle of which depends on the no of relative transistors distance between Output points.

Sufficiently Small duty cycle clock can save a lot area for counter design as it avoids Race Around condition, and 'J-K FF' can also be used, thus not always requiring Master – Slave configuration which can save a lot area (roughly half) and makes design compact.

The AND Gate is implemented by CVSL, which additionally saves on Static Power Dissipation as cross coupled transistors doesn't provide any current path, making it Low power with Compact design.

The UP counter is implemented in Verilog in Digital block.

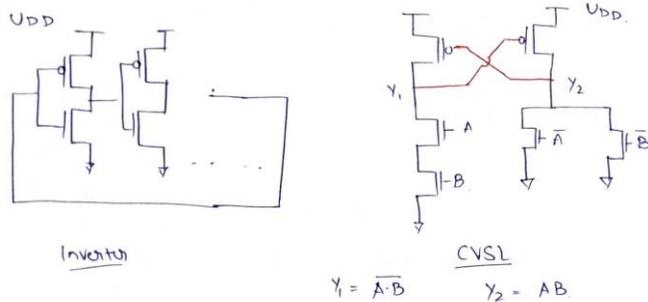


Figure 3 Transistor Level Design for Analog Block

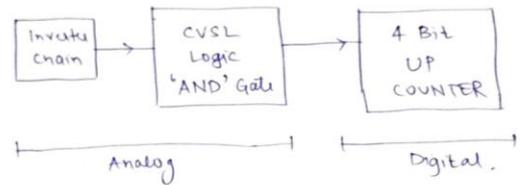


Figure 1 Block Level Implementation

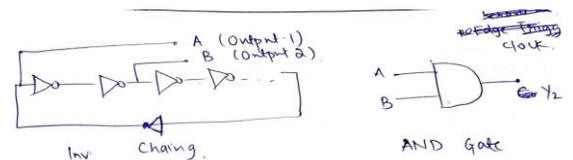


Figure 2 Logic Level Design for Analog Block

Waveforms

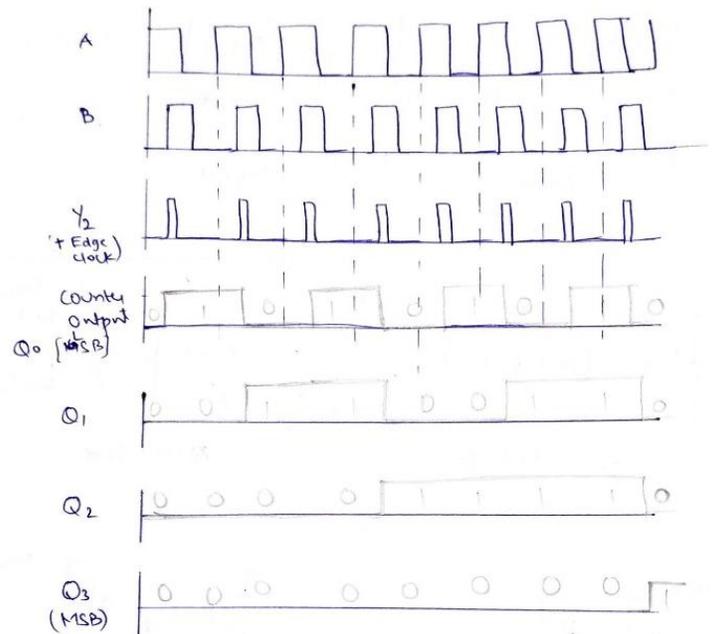


Figure 4 Output Waveforms