DESIGN OF 4 BIT COUNTER WITH CLOCK AS INVERTER CHAIN AND LOW POWER CVSL (Cascode Voltage Switch Logic)

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Abstract— **A 4 Bit UP Counter is 'Designed and Implemented' with clock being generated from Inverter chain circuit (Ring Oscillator) followed by Low Power Cascode Voltage Switch Logic 'AND' Gate to reduce Duty Cycle of Clock.**

Lower Duty Cycle clock allows Level triggered flip flop to be used, as it avoids Race around conditions. Conventional Master Slave configuration uses combination of two level triggered flip flops as an edge triggered Flip Flop, hence effectively half area in a single Flip Flop can be saved, increasing functionality for the same chip area.

Keywords—Ring Oscillator, CVSL AND Gate, Counter
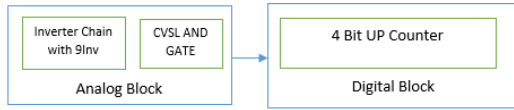
Fig 3: Output Waveforms

I. CLOCK GENERATION

Fig 1: Block level Diagram

First Block in Fig. 1 comprises of Inverter Chain Circuits comprising of 9 Inverters, which operates as Ring Oscillators with Frequency approx. 150Mhz.

Output of Ring Oscillator is taken as A. Another Output (B) is taken from (2 gates earlier) from the chain to get delayed same state. Both the output A,B are 'anded' to get a wave with lesser duty cycle, which can work as Low Duty Cycle Clock, the duty cycle of which depends on the no of relative transistors distance between Output points and no of transistors in chain. A bar and B bar required for CVSL are taken from prev. consecutive Inv stages of A and B Points.
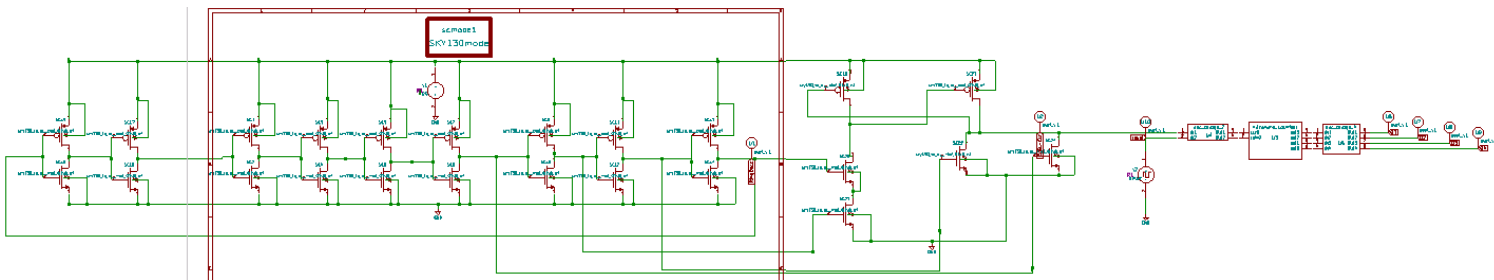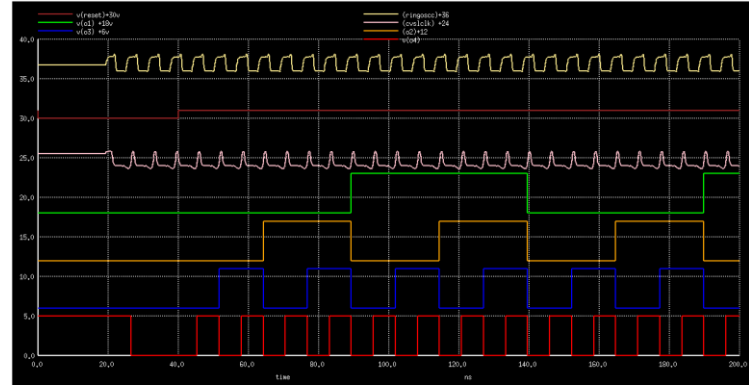
II. NEED OF LOW DUTY CYCLE

Sufficiently Small duty cycle clock can save a lot area for counter design as it avoids Race Around condition by satisfying $T_{clk} > T_{pdFF} > T_{on-clk}$, thus reqd T_{on-clk} can be achieved by CVSL AND Gate, and 'J-K FF' can also be used, thus not always requiring Master-Slave configuration which can save a lot area, and thereby reducing power also alongwith compact design.

III. CVSL AND GATE

The AND Gate is implemented by CVSL, which additionally not consumes Static Power as cross coupled transistors doesn't provide any current path , making it Low power with Compact design.

As can be seen from the Fig3: Output Waveforms, the Duty Cycle of output of CVSL AND Gate (3rd from top) is much lesser than that of Ring Osillator (top most waveform).

Fig 2: Schematics of Mixed Signal Design