

32-bit SRAM implementation in eSim using Skywater 130nm CMOS technology

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Abstract- Today, Static Random Access Memory (SRAM) has become a standard memory element of any Application Specific Integrated Circuit (ASIC), System-On-Chips (SoC), because they are fast, robust, nearly universally found on the same die with microcontrollers and microprocessors. This paper presents detailed implementation of 32 bit SRAM using eSim and SKY130 PDK. SRAM is much faster than DRAM (Dynamic RAM), so to utilize SRAM to the fullest we have the concept of caching the memory i.e we save the data in SRAMs on first load so that in the consecutive load time reduces drastically. SRAM can retain its stored information as long as power is supplied.

I. IMPLEMENTED CIRCUIT DETAILS

The structure of a 6 transistor SRAM cell which can store one bit of data is implemented in eSim using SKY130 PDK NMOS and PMOS transistors as show in Fig 1. The word and bit lines, wl and bl, are used to read and write from or to the cell. A 32-bit SRAM memory array is implemented, using 130nm CMOS technology and modular design approach. First, a 8 bit SRAM cell is build using eight 1 Bit SRAM. They are accessed by 3 bit address using a 3x8 decoder which is implemented in digital domain as shown in Fig 2.

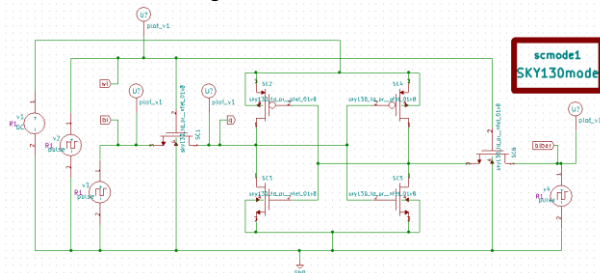


Fig. 1. Standard 6T SRAM Cell

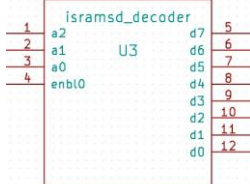


Fig. 2. Digital Block: 3x8 Decoder

1 bit RAM cell consists of data writer circuit, 6T RAM cell, pre-charge circuit and a sense amplifier all implemented in eSim as shown in Fig 3. The 3x8 decoder will be used to select the 1-bit RAM cell to which we want to perform the read/write operation.

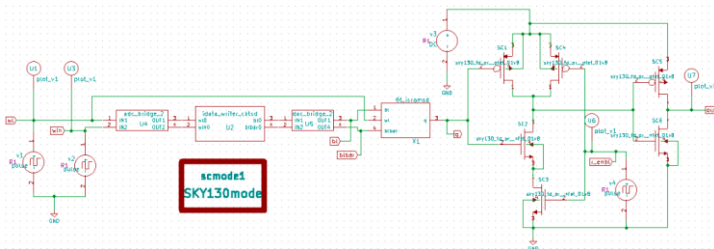


Fig. 3. Analog Block: 1 bit SRAM Cell implemented in eSim

Digital blocks i.e writer circuit and 5x32 decoder are implemented in Verilog (Ngveri) in eSim, whereas analog block are implemented in eSim as shown in Fig 4. After creation of all the symbols using sub-circuit feature, interconnection of the 5x32 decoder and the 1-Bit SRAMs will be

carried out as shown in the schematic to create the 32-Bit SRAM.

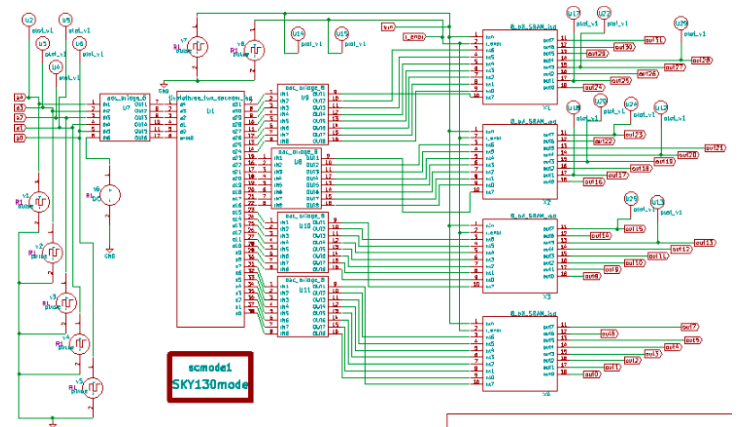


Fig. 4. 32 bit SRAM Mixed circuit implementation in eSim using Sky130 PDK

II. IMPLEMENTED WAVEFORMS

Fig. 5 depicts the transient waveforms for a 8 bit SRAM. Results are consistent with reference waveforms and Fig 5 depicts 32 bit SRAM waveforms for some outputs cases.

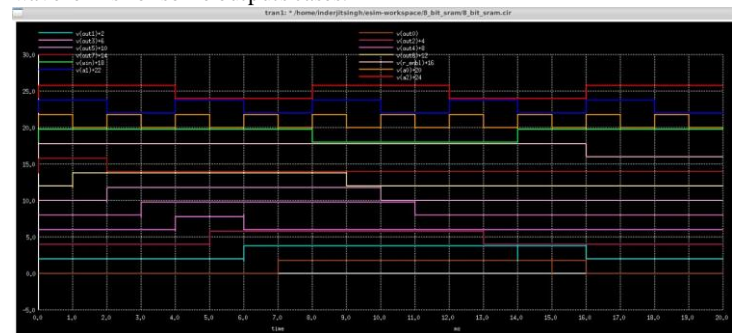


Fig. 5. Transient input and output waveforms of 8 bit SRAM

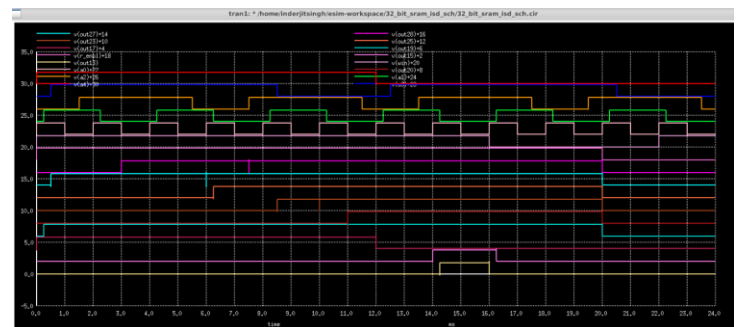


Fig. 6. Transient input and output waveforms of 32 bit SRAM

REFERENCES

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