Design and Implementation of 8 Bit SRAM

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Abstract- Static Random Access Memory (SRAM) is a static memory cell which is being used in various electronic devices. It is faster as compared to other memory cells and even consumes lesser power and is not required to be refreshed periodically. The application of this circuit can be a simple memory element, a Lookup table for an FPGA etc.
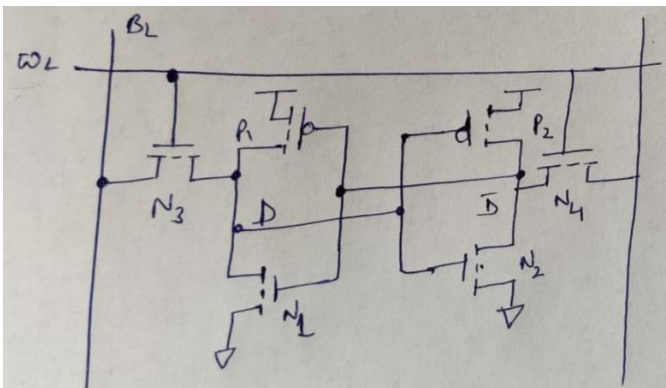
Keywords – 6T Memory Cell, Static RAM.
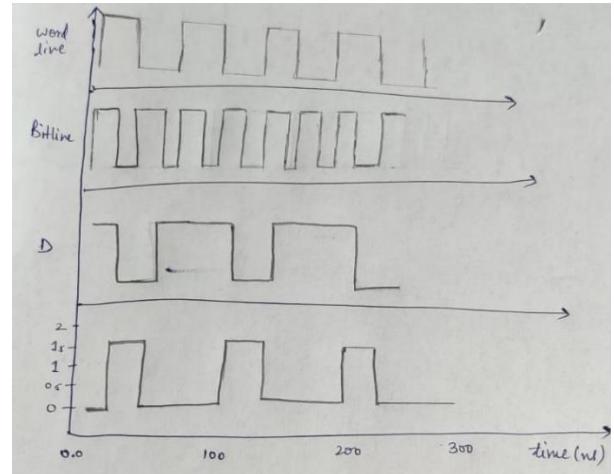
1. Introduction

The architecture of the 6T SRAM cell is shown in the figure 1. A basic 6T SRAM cell has two inverters connected back to back.

We will be using 8 of such circuits in order to get the 8 bits required for the implementation. This array of 1 bit RAM will be modified (read and write) using a decoder circuit. The decoder will be coded in Verilog and the SRAM will be made in Esim.

2. Reference Circuit

3. Reference Waveform

4. References

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