7T SRAM Cell with Peripheral Circuitry.

Mohammad Mudakir Fazili
dept. of Electronics and Communication Engineering
National Institute of Technology Srinagar
Srinagar, India
mudakirfazili@gmail.com

***Abstract*—Memory, the critical component of all computing devices, is essential in determining the system's efficiency. Conventionally, memory is categorized into two types based on its functionality: working memory and storage memory. In this initial report a 7T SRAM architecture is presented and is scaled to 32 Byte. Also, some of the peripheral circuitry is also presented. A mixed signal approach is taken: with SRAM being designed in spice and the peripheral circuitry being designed in verilog.**

***Index Terms*—Memory, Storage Memory, SRAM, Verilog**

I. Introduction

Memory devices represent 25% of the total semiconductor market which signifies the importance of memories in the modern-day world. With each passing day, the requirement for more and faster memories is increasing rapidly. Thus, the growing demand for low-cost memories has driven the technological advancement of new memory devices. In the this project,

1) A 7T SRAM will be designed.
2) All of its performance metrics will be calculated.
3) Scaling will be performed based on the performance metrics.
4) Peripheral circuitry will be designed in verilog.
5) All the circuits will be combined and a functional verification will be performed.

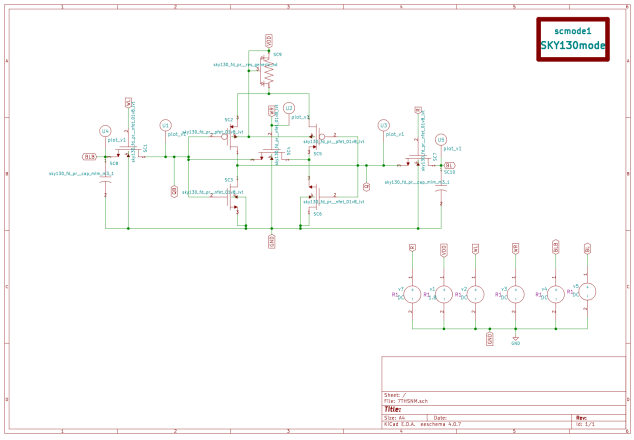

Fig. 1. Circuit Diagram of 7T SRAM.

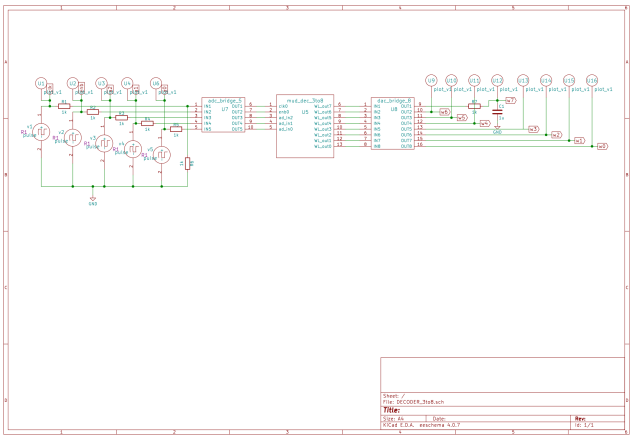

Fig. 2. Circuit Diagram of 3:8 Decoder.

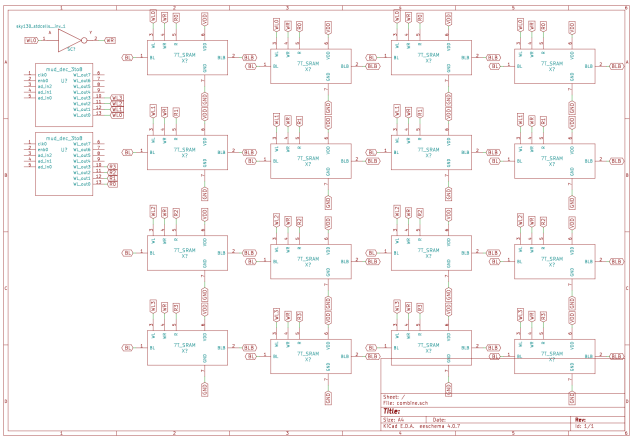

Fig. 3. Circuit Diagram of peripheral circuitry and 7T SRAM Cells.

References

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[2] Yu, Shimeng. Semiconductor Memory Devices and Circuits. CRC Press, 2022.