

6T SRAM Cell With Read and Write Operation

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ABSTRACT

6T static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. This report demonstrates the design of a 6 - Transistor Static RAM cell that stores 1bit of data and also explains its READ and WRITE operation, implementation of design, and explains the function of how it stores 1bit in a cell.

REFERENCE CIRCUIT DETAILS

SRAM, known as Static Random Access Memory also known as Read Write Memory has become a very crucial part of SOC's and ASIC. As the basic unit of SRAM is the SRAM cell, the need of SRAM cell is to perform stable and robust read/write operation in such a way that it consumes the least power and enhance the on-chip storage capacity. The given circuit demonstrates six transistor SRAM cell, out of which four transistors Q1, Q2, Q3, and Q4 forms a cross-coupled CMOS inverter, that itself becomes a memory. And remaining two nmos act as access transistors. These access transistors are connected to the bit line and bit line bar that are denoted by "BL & BLB". And word line here denoted by "WL" is connected to access transistors when the word line is set on, the access transistors can be accessed and similarly when a word line is set off the content of the memory comes set to hold state as the access transistors are turned off, and as a result, the data will remain unchanged in the cell, for the write operation bit line and bit line bar acts as input lines and for reading operation these lines would act as output lines. We would design this circuit using open-source SkyWater 130nm PDKs.

IMPLEMENTED CIRCUIT

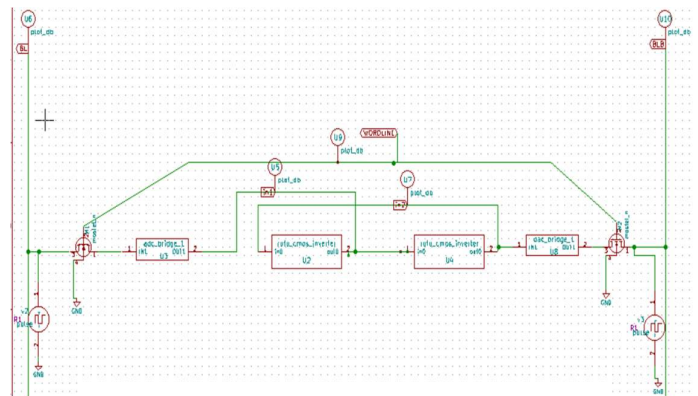


Fig 1: Implemented circuit diagram

IMPLEMENTED WAVEFORMS

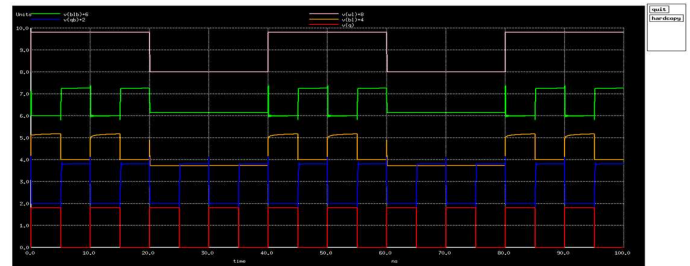


Fig 2: Waveform for Read operation

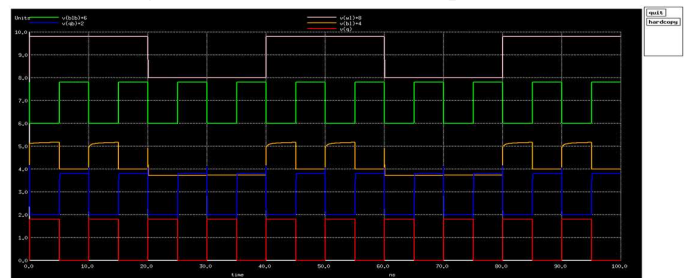


Fig 3: Waveform for Write operation

REFERENCES

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