Design of 3-Bit Flash ADC using Inverter Threshold Comparator

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***Abstract*—Analog to Digital Converter (ADC) converts time continuous physical signal to digital number. In simple words, ADC converts analog signals in to digital signals that can be used by electronic circuits. In this paper a 3-bit Flash ADC will is designed and implemented using comparator circuit called Inverter Threshold Comparator (ITC). The Sample & Hold circuit for ADC is implemented using Transmission Gate Switch (TGS). The Priority encoder is implemented as a Digital Circuit and coded using Verilog. The design is implemented using e-sim tool.**

I. CIRCUIT DETAILS

Transmission Gate Switch: Transmission Gate switch is designed for the following specifications. Input frequency <= 20 KHz, Input Voltage range = 0 to 1V, VDD = 1V and Sampling frequency = 800 KHz.

	PMOS	NMOS	Capacitor = 5.0412 pF
W	15u	15u	100
L	0.45u	0.45u	25
MF	---	---	1

Table I. Design Table of TGS

Latch			
en	D3	D2	D1
0	D3	D2	D1
1	Y3	Y2	Y1

Table II. Truth Table of Latch

Inverter Threshold Comparators (ITC): Seven Inverter Threshold Comparators are designed for following specifications. VDD = 1V, Reference Voltages (Threshold Voltages): 0.2V, 0.3V, 0.4V, 0.5V, 0.6V, 0.7V, 0.8V

ITC	Vth(mV)	PMOS		NMOS	
		W(u)	L(u)	W(u)	L(u)
1st	202.542	1	16.5	50	0.45
2nd	303.39	1	3	4	0.45
3rd	400.39	1	0.3	5	0.3
4th	500.8	1	0.15	9	0.3
5th	602.5	3	0.15	1	0.15
6th	700	50	0.15	1	3
7th	804.23	30	0.15	1	60

Table III. Design Table of ITCs

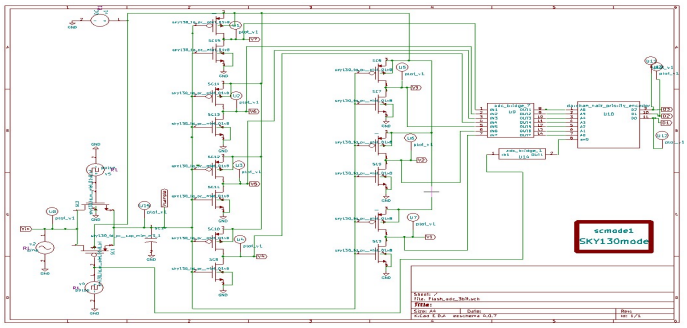
Priority Encoder with Latch: The priority encoder is designed to convert the output of seven comparators into 3-bit digital output. The output of encoder is given to latch and the final output is enabled only during the hold period of Sample and Hold circuit.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	Y_3	Y_2	Y_1
1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0	0	1
1	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	0	1	1
1	1	1	0	0	0	0	1	0	0
1	1	0	0	0	0	0	1	0	1
1	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	1	1

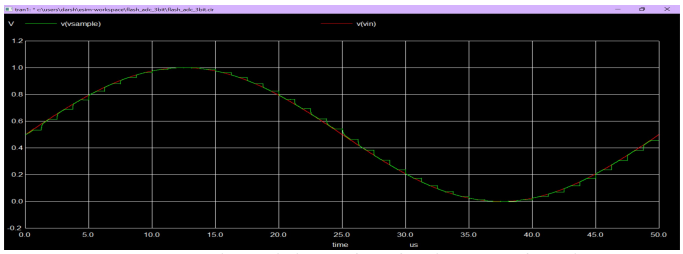
Table IV. Truth Table of the encoder

NOTE: In the literature survey report reference waveforms are mentioned for Ramp Wave input just to show the expected waveform of ADC but in implementation Sine waveform is used to make frequency analysis as it is difficult to use ramp wave for frequency analysis. But the required output is obtained

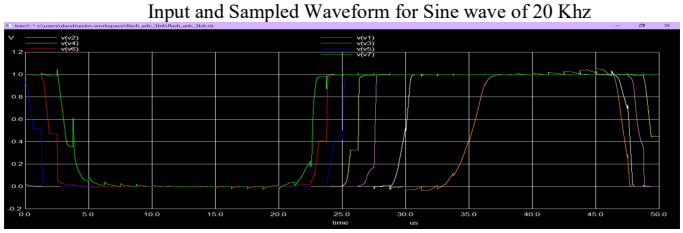
II. IMPLEMENTED CIRCUIT



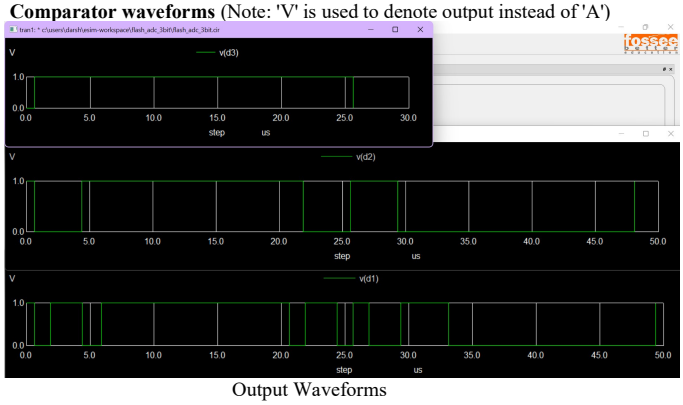
III. IMPLEMENTED WAVEFORMS



Input and Sampled Waveform for Sine wave of 20 Khz



Comparator waveforms (Note: 'V' is used to denote output instead of 'A')



Output Waveforms

REFERENCES

[1] Harisha, Satheesh Rao," Design of 3-bit Flash ADC using Inverter Threshold Comparator in 45 nm CMOS Technology",2017 International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT)

[2] Meng-Tong Tan, Joseph S. Chang and Yit-Chow Tong," A Process-Independent Threshold Voltage Inverter-Comparator for Pulse Width Modulation Applications"