

Design of Charge Pump Phase Locked Loop in Sky130nm

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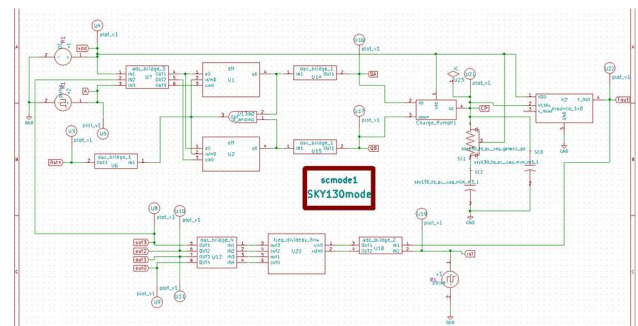
Abstract—This paper proposes the implementation of Phase Locked Loop (PLL) using CMOS technology. PLL is a Mixed block which uses a Phase Frequency Detector (PFD) and Divide by N network as Digital Block and Charge Pump, Low Pass Filter and Voltage Control Oscillator as Analog Block. PLL are used to generate output clock that is well synchronized with reference clock both in terms of phase and frequency. It has typical applications such as clock generation for Microprocessors or Frequency synthesizers used in mobile phone. This Mixed signal circuit has been redesigned and simulated with Sky130 nm process node using eSim EDA tool developed by FOSSEE IIT Bombay.

I. PLL CIRCUIT DETAILS

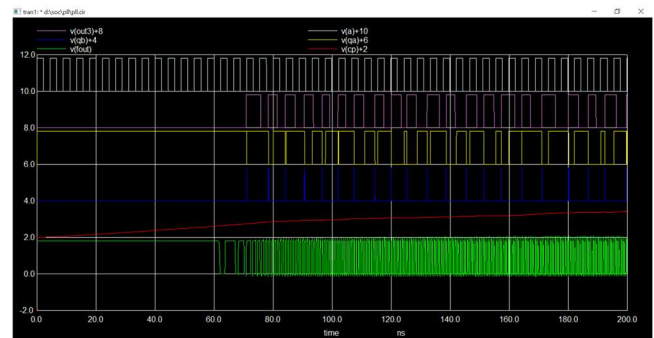
Phase Locked Loop Block diagram is shown in section II. It consists of 1st input digital block i.e. Phase frequency detector which will compare reference i.e input frequency and phase with output frequency and phase and provides two output signals named V(up) and V(down). If V_{in} i.e $V(a)$ has frequency more than V_{out} or if V_{in} is leading V_{out} then V(up) continues to produce pulses whose width is proportional to $\phi_{in} - \phi_{out}$ and V(down) doesn't. Similarly if V_{out} is leading V_{in} or It has more frequency than V_{in} then V(down) continues to generate pulses while V(up) remains at 0. These V(qa) i.e. UP and V(qb) Down signals are then used to activate charge pump to pump proportional current I_o in C_p capacitor to produce control voltage V_{ctrl} i.e (Vcp). As this V_{ctrl} will have both AC and DC components, It is then passed through the Low pass filter to give DC V_{ctrl} voltage. This control voltage is then applied as an input voltage to VCO i.e. Voltage controlled Oscillator. VCO produces a frequency which is proportional to V_{ctrl} voltage. As VCO produces a frequency i.e. N times input frequency $f_{out} = N * f_{in}$, It is then passed through divide by N network to get $f(V_{out3}) = f_{out}/N$ which is then fed back to PFD where it compares it with reference input frequency f_{in} .

Simulated PLL waveforms at different blocks output are shown in section III. As soon as V_{in} is applied PLL switches from free running state to capture state here we can observe Vup and Vdown pulses are generated with corresponding V_{ctrl} to correct the phase and frequency shift between $V_{in}(f_{in})$ and $V_{out}(f_{out}/N)$. With this V_{ctrl} , VCO produces a frequency that

tries to track the f_{in} . Once $f_{out} = N * f_{in}$ and $\phi_{out} = \phi_{in}$, V_{ctrl} becomes almost constant and PLL enters into locked state. Pll block diagram



II. PLL WAVEFORMS



REFERENCES

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- [2] Behzad Razavi Reference Book- "Design of Analog CMOS Integrated circuits" *Mc Graw Hil Education*, 2ed edition.
- [3] Paras Gidd, Git-hub Repo, "https://github.com/parasgidd/avsdpll_3v3"