

Sequence Detector

Arpit Kumar

Department of Electronics and Communication Engineering

Dayananda Sagar College of Engineering

Bangalore, India

arpitk2001kumar@gmail.com

Abstract—This Mixed Signal Project aims to implement a sequence detector. Analog signals will be converted to binary signals using a flash ADC. This binary signal will be used as input for the sequence detecting FSM. The FSM will be designed using an HDL.

Keywords—Mixed Signal, Flash ADC, Sequence Detecting, FSM

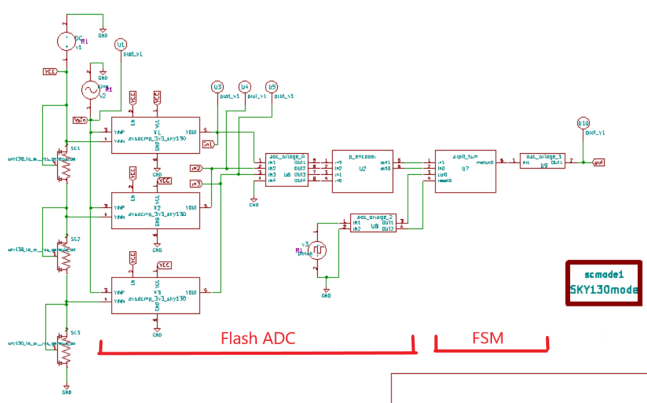
I. REFERENCE CIRCUIT DETAILS

The circuit consists of comparators (from the sky130 library), a priority encoder and an FSM. The comparators and the priority encoder come together to form a flash ADC. The output of the flash ADC is fed to the FSM to detect a particular sequence. This FSM is slightly different from your typical FSM as it has a 2-bit input but the functionality remains the same. The sequence we are trying to detect is 11 - 10 - 01. This tells us when the signal starts falling in value (amplitude).

The flash ADC takes in the analog signal and a reference voltage (for comparison). The different comparators get different reference voltages due to the voltage divider. This helps us to assign binary values to different voltage levels.

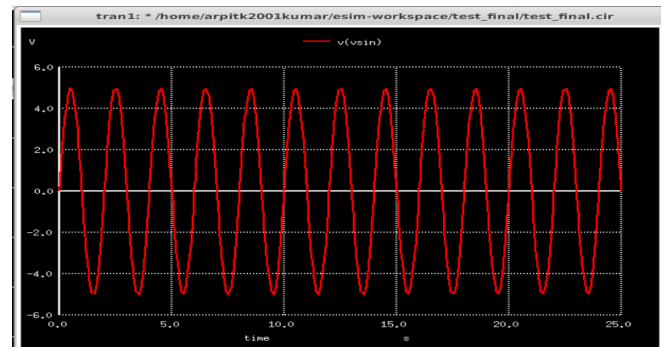
The FSM has 3 states and gives output as one once all the states are called in order.

II. IMPLEMENTED CIRCUIT SCHEMATIC

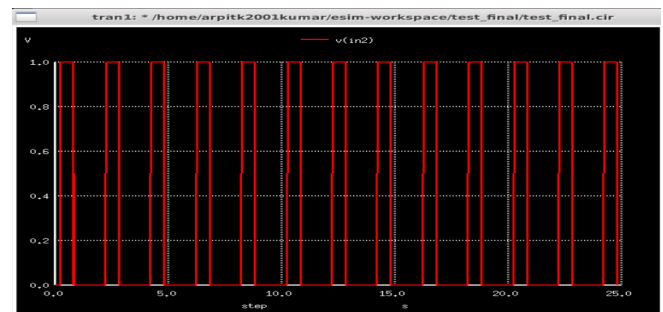


III. IMPLEMENTED WAVEFORMS

Here we are given a sine wave as an input. Ideally, the FSM will give output '1' when the sine wave goes down.



Here is the output of the topmost comparator. we can see that it outputs '1' when the sine amplitude exceeds the reference voltage and '0' otherwise.



Please note that all the components are working correctly. The only issue is with the voltage divider. Due to the resistance value, all comparators are getting the same reference voltage. Therefore a sequence is not being generated.

IV. REFERENCES

<https://www.analog.com/en/analog-dialogue/articles/analogue-to-digital-converter-architectures-and-choices.html>